

P3A1604UK

4-bit Dual Supply Translating Transceiver; Auto Direction Sensing

Rev. 1.1 — 27 June 2025

Product data sheet

Document information

Information	Content
Keywords	P3A1604UK, data sheet, dual supply translating transceiver
Abstract	The P3A1604UK is a 4-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation.



1 General description

The P3A1604UK is a 4-bit, dual supply translating transceiver with auto direction sensing that enables bidirectional voltage level translation. It features four 1-bit input-output ports (A and B), one output enable input (OE), and two supply pins (V_{CCA} and V_{CCB}). V_{CCA} can be supplied at any voltage between 0.72 V and 1.98 V. V_{CCB} can be supplied at any voltage between 1.62 V and 3.63 V. This flexibility makes the device suitable for translating between any of the voltage nodes (0.8 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V). Pins A and OE are referenced to V_{CCA} and pin B is referenced to V_{CCB} . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state.

2 Features and benefits

- Auto direction sensing and bidirectional voltage level translation
- Wide supply voltage range:
 - V_{CCA} : 0.72 V to 1.98 V and V_{CCB} : 1.62 V to 3.63 V
- No power-sequencing required
- Maximum data rate (DDR) per bit
 - Open-drain: 6.8 Mbit/s (3.4 MHz)
 - Push-pull: 40 Mbit/s (20 MHz)
- Support I3C/I2C/SMBus/SPI/UART interfaces
- Longer one-shot pulse for driving larger capacitive loads with much reduced ringing and overshoot
- A-side and OE inputs accept voltages up to 1.98 V
- B-side inputs accept voltages up to 3.63 V
- Electrostatic discharge (ESD) protection:
 - Human body model (HBM) JESD22-A114E Class 2 exceeds 2000 V
 - Charged device model (CDM) JESD22-C101E exceeds 500 V
- I/O latch-up current 100 mA, JESD 78
- Package:
 - WLCSP12 (1.405 mm x 1.055 mm, 0.35 mm pitch)
- Specified from -40 °C to +125 °C

3 Applications

- Mobile
- I3C/I2C/SMBus
- SPI
- Server

4 Ordering information

Table 1 describes the ordering information for P3A1604UK.

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
P3A1604UK	4U ^[1]	WLCSP12	Wafer Level Chip Scale Package; 12 balls with 0.35 mm pitch; 1.405 mm x 1.055 mm	SOT2063-4

[1] “X4” for engineering sample and “4U” for production

4.1 Ordering options

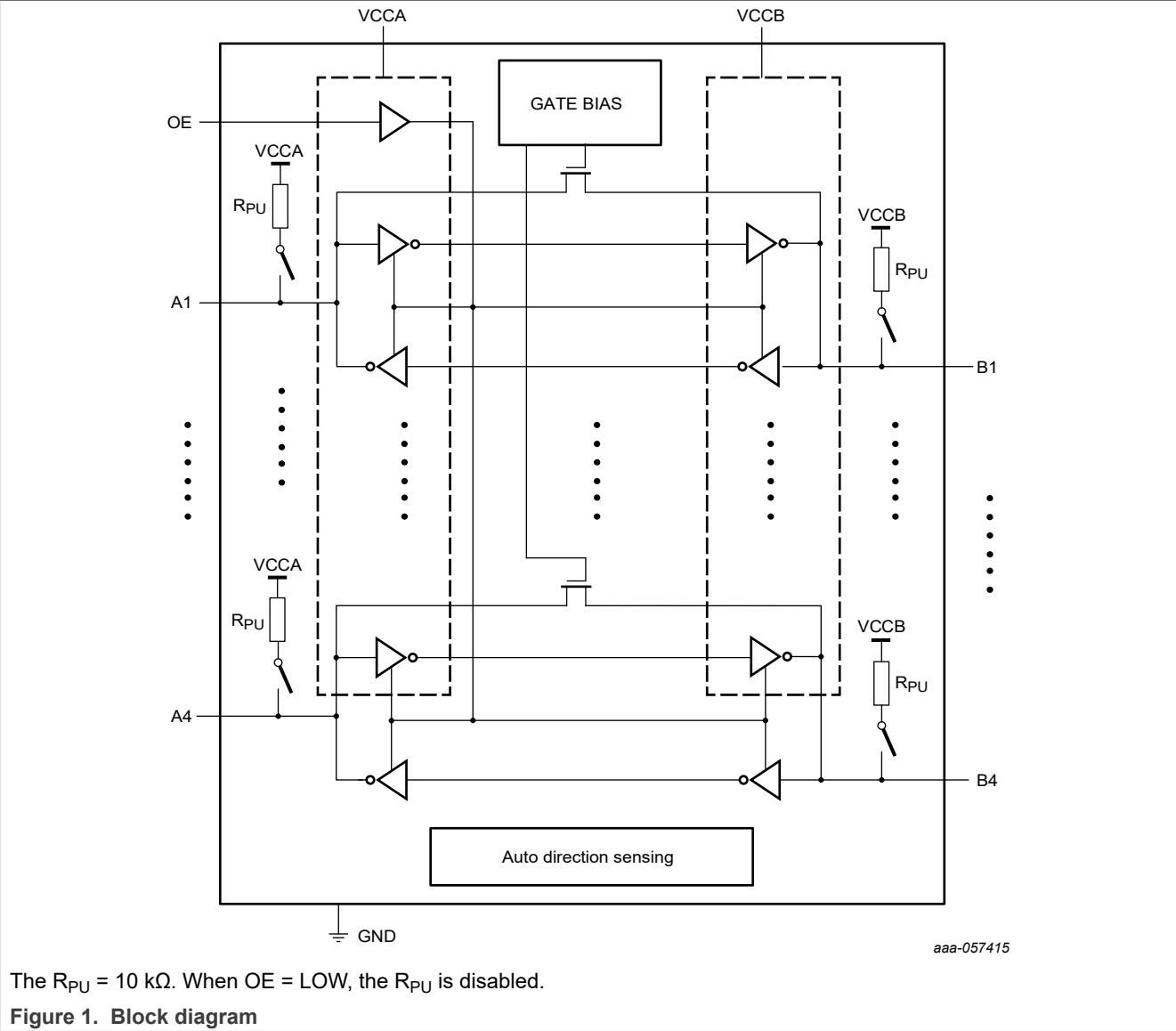
Table 2 describes the ordering options for P3A1604UK.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3A1604UK	P3A1604UKAZ	WLCSP12	Reel 7" q1/t1 *special mark chips dp	4400	T _{amb} = -40 °C to +125 °C

5 Block diagram

Figure 1 shows the labeled block diagram of P3A1604UK.



The R_{PU} = 10 kΩ. When OE = LOW, the R_{PU} is disabled.

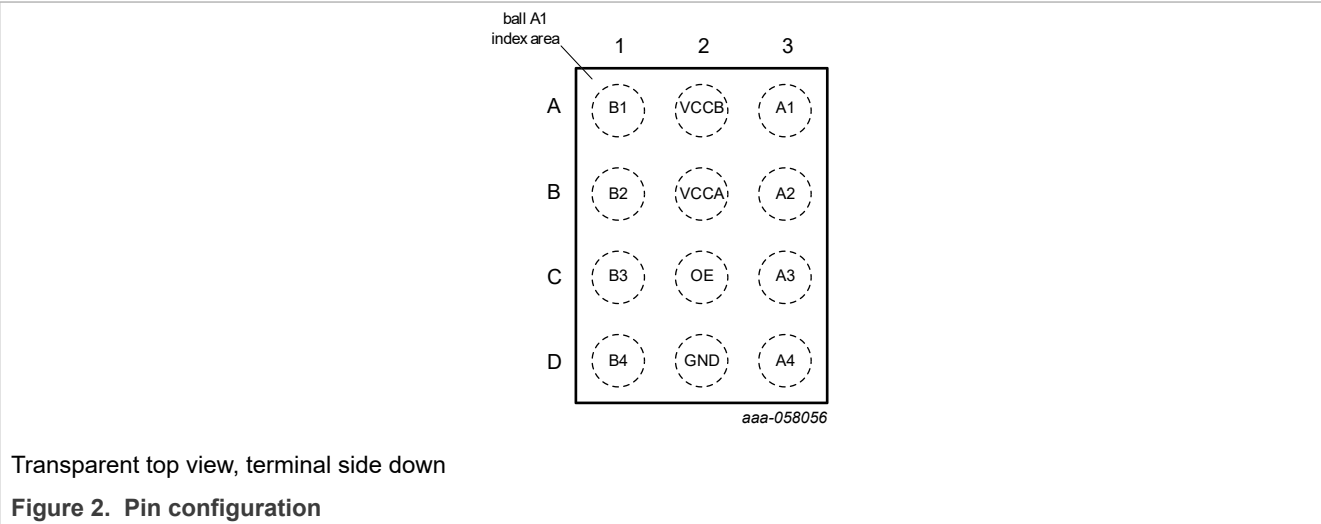
Figure 1. Block diagram

6 Pinning information

This section provides the pin configuration and description of the P3A1604UK package.

6.1 Pinning

Figure 2 shows the pinning for P3A1604UK.



6.2 Pin description

Table 3 provides detailed description of various pins on P3A1604UK.

Table 3. Pin description

Symbol	Pin	Description
B1	A1	Data input or output (referenced to V _{CCB})
V _{CCB}	A2	Supply voltage B
A1	A3	Data input or output (referenced to V _{CCA})
B2	B1	Data input or output (referenced to V _{CCB})
V _{CCA}	B2	Supply voltage A
A2	B3	Data input or output (referenced to V _{CCA})
B3	C1	Data input or output (referenced to V _{CCB})
OE	C2	Output enable input (active High, referenced to V _{CCA})
A3	C3	Data input or output (referenced to V _{CCA})
B4	D1	Data input or output (referenced to V _{CCB})
GND	D2	Ground
A4	D3	Data input or output (referenced to V _{CCA})

7 Functional description

Refer to Figure 1.

7.1 Architecture

The architecture of this device does not require an extra input signal to control the direction of data flow from A to B or B to A.

The P3A1604UK is a “switch” type voltage translator using two key circuits to enable voltage translation:

- 1. A pass-gate transistor (N-channel) that ties the ports together.
- 2. An output edge-rate one-shot accelerator that detects and accelerates rising and falling edges on the I/O pins.

[Table 4](#) describes the function for different OE and I/O states.

Table 4. Function table

Supply voltage		Input ^[1]	Input/output ^[1]	
V _{CCA}	V _{CCB}	OE	A	B
0.72 V to 1.98 V and V _{CCA} ≤ V _{CCB}	1.62 V to 3.63 V	L	Z	Z
0.72 V to 1.98 V and V _{CCA} ≤ V _{CCB}	1.62 V to 3.63 V	H	Input or output	Output or input
GND ^[2]	GND ^[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = donot care; Z = high-impedance OFF-state.
[2] When either V_{CCA} or V_{CCB} is at the GND level, the device goes into power-down mode.

7.2 Input driver requirements

As the P3A1604UK is a switch-type translator, the properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (t_{THL}), and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume that a driver with an output impedance below 50 Ω is used.

7.3 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. The P3A1604UK has a longer one-shot pulse for driving larger capacitive loads.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on P3A1604UK PCB layouts. The length of the PCB trace is such that the round-trip delay of any reflection is within one-shot pulse duration. This one-shot pulse duration is approximately 10 ns to 30 ns. It ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

If required, a series resistor on the signal path is recommended. For more details, see [Section 8.1](#).

7.4 Power up

During operation, V_{CCA} must never be higher than V_{CCB}. However, during power up, V_{CCA} ≥ V_{CCB} does not damage the device. So, either power supply can be ramped up first.

It requires 50 μs max after V_{CCB} reached regulating voltage and 4 μs max after V_{CCA} reached regulating voltage for the internal circuit setup correctly.

There is no special power up sequencing required. The P3A1604UK includes circuitry that disables all output ports when either V_{CCA} or V_{CCB} is switched off.

7.5 Enable and disable

An output enable input (OE) is used to enable/disable the device. The OE is referenced to V_{CCA} . Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (ten) indicates the amount of time the user must allow for one-shot circuitry to become operational after OE is taken HIGH. Before the ten (3 μ s max), the I/O status is ignored.

To ensure the high-impedance OFF-state during power up or power down, pin OE is tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

7.6 Pull-up or pull-down resistors on I/O lines

The A port I/O has an internal 10 k Ω pull-up resistor to V_{CCA} . The B port I/O has an internal 10 k Ω pull-up resistor to V_{CCB} . If a smaller value of pull-up resistor is required, add an external resistor in parallel to the internal 10 k Ω . This pull-up resistor affects the VOL level. When OE goes LOW, the internal pull-ups of the P3A1604UK are disabled. For open-drain signal, at least one side pull-up R on either A side or B side I/O pin is required. The pull-down resistor is not recommended to avoid incorrect I/O logic level.

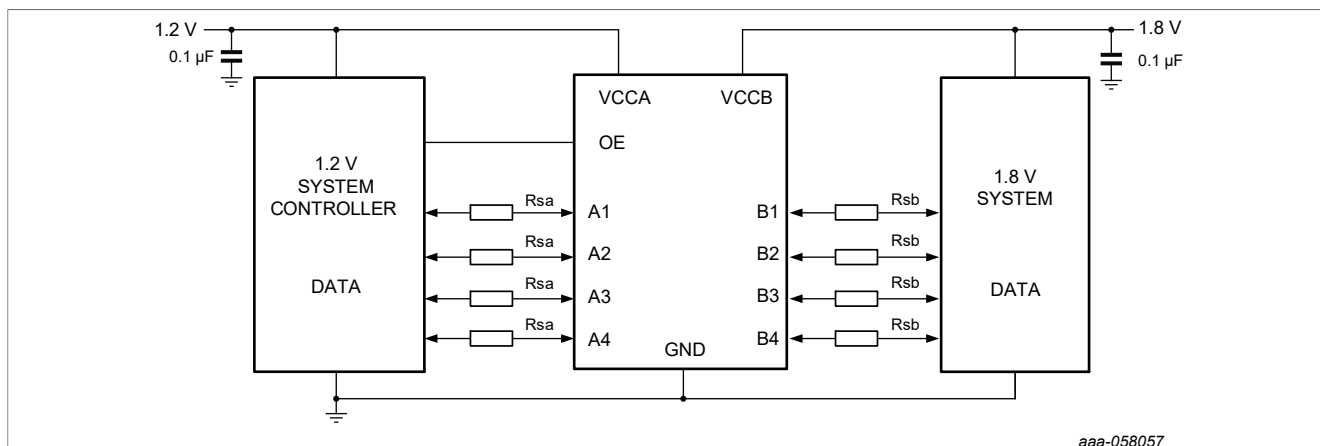
8 Application information

This section explains the applications and architecture associated with P3A1604UK.

8.1 Applications

P3A1604UK can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device can support both open-drain and push-pull interfaces like I3C/I2C/SMBus/SPI/UART. See [Figure 3](#) for the typical application circuit.

If the PCB trace length is too long (> 30 cm) or the parasitic impedance is too large, the I/O signal may overshoot/undershoot or lead to oscillation. A series resistor (R_s) is recommended on each I/O pin to reduce the overshoot/undershoot and avoid the oscillation. The recommended value is 30 Ω . Adjust the R_s value for optimized signal integrity is required based on with different wire lengths and PCB parasitic R/L/C. Ensure that the series resistor value is not too high to affect the VOL level.



V_{CCA} range: 0.72 V to 1.98 V, V_{CCB} range: 1.62 V to 3.63 V.

R_{sa} and R_{sb} ($\sim 30 \Omega$) are optional based on the signal integrity.

For open-drain signal, at least one side pull-up R on either A side or B side I/O pin is required.

Figure 3. Typical application circuit

8.2 Architecture

Figure 4 describes the architecture of P3A1604UK design for both push-pull and open-drain mode. To meet these requirements, the architecture uses:

1. Edge-rate accelerator circuitry (for both high-to-low and low-to-high)
2. N-channel Pass gate transistor
3. Pull-up resistor (to provide DC-bias and drive capabilities)

The design is directionless and does not need a direction control signal. The implementation supports both low-speed open-drain operation and high-speed push-pull operation. The N-channel pass device T5 is on only during the low input cycle and is off during the high input cycle.

Data transmission from A-ports to B-ports: During a rising edge and A port voltage = V_{IH} , OS1 (one-shot) and OS2 (one-shot) turn on both PMOS transistor T1 and T2 respectively for a short duration. This operation reduces the low to high transition time. The T1 duration is around 10 ns. The T2 duration is around 10 ns min to 30 ns max, which depends on the CLB (load capacitance on the B side). Similarly, during a falling edge, when transmitting data from A to B and voltage = V_{IL} , both OS3 and OS4 one-shots turn on the N-channel transistor T3 and T4 for a short duration, which speeds up the high to low transition.

Data transmission from B-ports to A-ports: During a rising edge and B port voltage = V_{IH} , OS1 (one-shot) and OS2 (one-shot) turn on both PMOS transistor T1 and T2 respectively for a short duration. This operation reduces the low to high transition time. The T2 duration is around 10 ns. The T1 duration is around 10 ns min to 30 ns max, which depends on the CLA (load capacitance on the A side). Similarly, during a falling edge, when transmitting data from B to A and voltage = V_{IL} , both OS3 and OS4 one-shots turn on the N-channel transistor T3 and T4 for a short duration, which speeds up the high to low transition.

The internal pull-up resistors R_{upA} and R_{upB} are typically of the value of 10 k. Switches S1 and S2 control the resistors R_{upA} and R_{upB} respectively. The input signal and OE control their respective switches S1 and S2.

- Pull-up resistors are connected only when the switches are closed.
 - The switches are closed only when the input signal is High and OE enabled.
- Pull-up resistors are disconnected when the switches are open. Any one of the conditions has the switch open:
 - the respective input signal is low.

- the OE input signal is low.

For push-pull application, the external pull-up resistors are not required since at least one side is driven with a clear high or low state.

For open-drain application, at least one external pull-up resistor is required for pulling signal A from low state to high state. The external pull-up resistor can be either on A side or B side. The rising time can be estimated with $R_{up_ext} \times (C_{LA} + C_{LB}) + \text{one-shot time} (\sim 10 \text{ ns})$. Here, the R_{up_ext} is an external pull-up resistor and C_{LA} is the total load capacitance on the A side. C_{LB} is the total load capacitance on the B side.

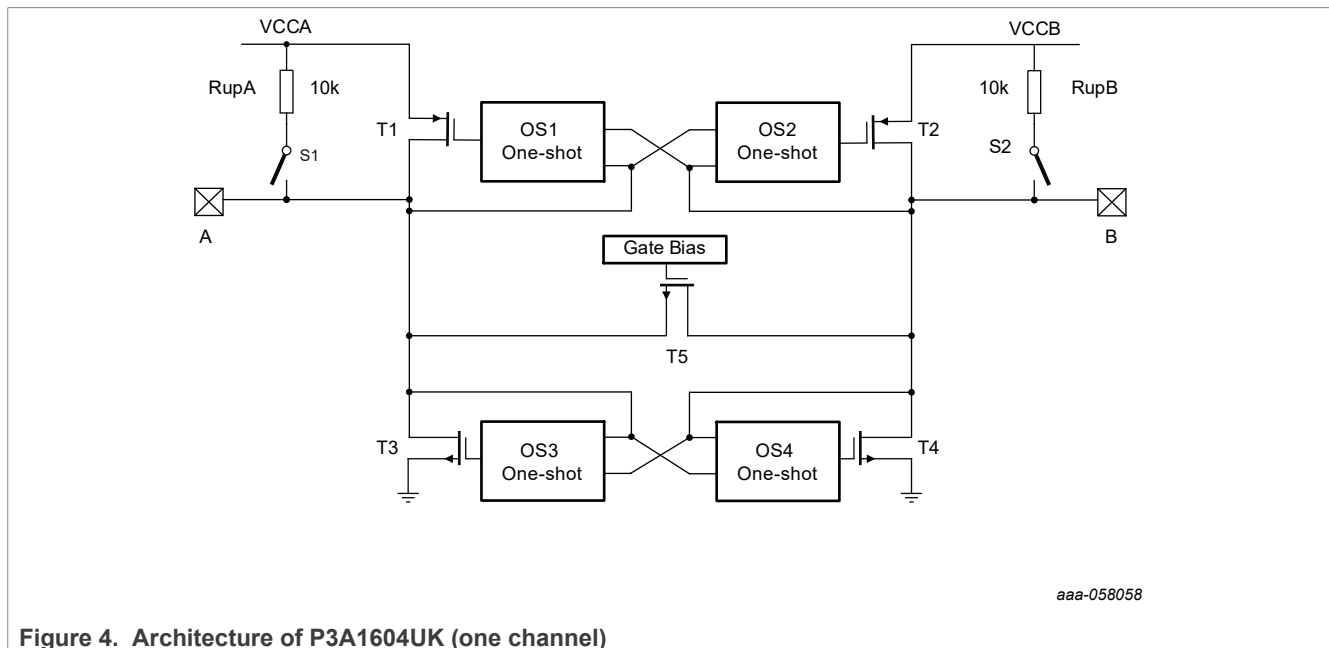


Figure 4. Architecture of P3A1604UK (one channel)

9 Limiting values

[Table 5](#) describes the limiting values of P3A1604UK.

Table 5. Limiting values

This table is in accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CCA}	Supply voltage A	V _{CCA} ≤ V _{CCB}	[1]	-0.5	+2.5	V
V _{CCB}	Supply voltage B		[1]	-0.5	+4.2	V
V _I	Input voltage	A port and OE input		-0.5	+2.5	V
		B port		-0.5	+4.2	V
V _O	Output voltage	Active mode				
		A or B port	[2] [3]	-0.5	V _{CCO} + 0.5	V
		Power-down or 3-state mode				
		A port		-0.5	+2.5	V
		B port		-0.5	+4.2	V
T _{stg}	Storage temperature			-65	+150	°C

[1] The minimum input and minimum output voltage ratings can exceed if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] $V_{CCO} + 0.5\text{ V}$ cannot exceed the associated V_{CCO} maximum limiting value.

10 Thermal characteristics

Table 6 provides the thermal characteristics of P3A1604UK.

Table 6. Thermal resistance information^{[1][2]}

Symbol	Parameter	Value (type)	Unit
R θ JA	Junction to ambient	77.9	°C/W
ψ JT	Junction to top characterization	9.3	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] The thermal test board meets JEDEC specification for this package (JESD51-9).

11 Recommended operating conditions

Table 7 describes the recommended operation conditions for P3A1604UK.

Table 7. Recommended operating conditions^[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CCA}	Supply voltage A	V _{CCA} ≤ V _{CCB} & 1.98 V	[2]	0.72	1.98	V
V _{CCB}	Supply voltage B			1.62	3.63	V
VI_EN	OE input voltage			-0.3	V _{CCA} +0.3	V
T _{amb}	Ambient temperature			-40	+125	°C
T _J	Junction temperature		[3]	-40	+125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	A or B port; push-pull driving				
		V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 1.62 V to 3.63 V	[2]	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] V_{CCA} must be less than or equal to V_{CCB} and 1.98 V.
[3] The TJ limits are supported by proper thermal PCB design taking the power consumption and the thermal resistance into account.

12 Static characteristics

Section 12 describe the static characteristics of P3A1604UK.

Table 8. Static characteristics

At recommended operating conditions, voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	HIGH-level input voltage	A port				
		V _{CCA} = 0.72 V to 0.9 V; V _{CCB} = 1.62 V to 3.63 V	V _{CCA} -0.2			V
		V _{CCA} = 0.9 V to 1.98 V;	0.65 x V _{CCA}			V

4-bit Dual Supply Translating Transceiver; Auto Direction Sensing

Table 8. Static characteristics...continued

At recommended operating conditions, voltages are referenced to GND (ground = 0 V); $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{CCB} = 1.62\text{ V}$ to 3.63 V ; & $V_{CCA} \leq V_{CCB}$				
		B port				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V ; & $V_{CCA} \leq V_{CCB}$	$0.65 \times V_{CCB}$			V
		OE input				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V ; & $V_{CCA} \leq V_{CCB}$	$0.65 \times V_{CCA}$			V
V_{IL}	LOW-level input voltage	A or B port				
		$V_{CCA} = 0.72\text{ V}$ to 0.9 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V ; [1]	-		$0.25 \times V_{CCA}$	V
		$V_{CCA} = 0.9\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V ; & $V_{CCA} \leq V_{CCB}$ [1]	-		$0.35 \times V_{CCA}$	V
		OE input				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V ; & $V_{CCA} \leq V_{CCB}$	-		$0.35 \times V_{CCA}$	V
V_{OHA}	HIGH-level output voltage	$I_O = -10\text{ }\mu\text{A}$				
		$V_{CCB} = 1.62\text{ V}$ to 3.63 V ; $V_I \geq 0.65 \times V_{CCB}$ [2]				
		$V_{CCA} = 0.72\text{ V}$ to 0.9 V [2]	$0.70 \times V_{CCA}$		-	V
		$V_{CCA} = 0.9\text{ V}$ to 1.98 V ; & $V_{CCA} \leq V_{CCB}$ [2]	$0.75 \times V_{CCA}$		-	V
V_{OHB}	HIGH-level output voltage	$I_O = -10\text{ }\mu\text{A}$				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V ; $V_I \geq 0.65 \times V_{CCA}$ [2]	$0.75 \times V_{CCB}$		-	V
V_{OL}	LOW-level output voltage	A or B port; $I_O = 1\text{ mA}$ [2] [3]				
		$V_I = 0.15\text{ V}$; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V	-		0.30	V
I_I	Input leakage current	OE; OE = 0 V or V_{CCA} ; $V_I = 0\text{ V}$ or V_{CCI} ; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V	-		1	μA
I_{OZ}	OFF-state output current	A or B port, OE = 0 V; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V [2]	-		2	μA

Table 8. Static characteristics...continued

At recommended operating conditions, voltages are referenced to GND (ground = 0 V); $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	Supply current	$V_{CCA} = 0\text{ V}$ or $V_{CCB} = 0\text{ V}$			3	μA
		OE = V_{CCA} , $V_I = 0\text{ V}$ or V_{CCI} ; $I_O = 0\text{ A}$ [4]				
		ICCA				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V	-		5	μA
		$V_{CCA} = 1.98\text{ V}$; $V_{CCB} = 0\text{ V}$	-		5	μA
		$V_{CCA} = 0\text{ V}$; $V_{CCB} = 3.63\text{ V}$	-		-5	μA
		ICCB				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V	-		15	μA
		$V_{CCA} = 1.98\text{ V}$; $V_{CCB} = 0\text{ V}$	-		-15	μA
		$V_{CCA} = 0\text{ V}$; $V_{CCB} = 3.63\text{ V}$	-		15	μA
		ICCA + ICCB				
		$V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 1.62\text{ V}$ to 3.63 V	-		20	μA
C_I	Input capacitance	OE input; $V_{CCA} = 1.2\text{ V}$; $V_{CCB} = 3.3\text{ V}$	-	2	-	pF
C_{IO}	Input/output capacitance	A port [5]	-	7	-	pF
		B port [5]	-	5.5	-	pF

[1] V_{IL} of A and B port is the value with respect to V_{CCA} .

[2] V_{CCO} is the supply voltage associated with the output.

[3] This spec has more margin. The R_{on} (resistance between input and output at low stage) max = $50\text{ }\Omega$. The equation for V_{OL} is $V_{OL} = V_i + I_o * R_{on}$.

[4] V_{CCI} is the supply voltage associated with the input.

[5] The C_{IO} is defined when A port and B port are isolated.

13 Dynamic characteristics

Table 9 describes the dynamic characteristics of P3A1604UK.

Table 9. Dynamic characteristics for temperature range $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ [1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7; for waveform see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		V _{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
V _{CCA} = 0.8 V ± 10 %								
t _{PHL}	HIGH to LOW propagation delay	A to B			6		5	ns

4-bit Dual Supply Translating Transceiver; Auto Direction Sensing

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for waveform see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions		V _{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	A to B			8		7	ns
t _{PHL}	HIGH to LOW propagation delay	B to A			5		4	ns
t _{PLH}	LOW to HIGH propagation delay	B to A			2		2	ns
t _{en}	Enable time	OE to A; B			3		3	µs
t _{dis}	Disable time	OE to A; no external load	^[2]		0.4		0.4	µs
		OE to B; no external load	^[2]		0.4		0.4	µs
		OE to A			0.8		0.8	µs
		OE to B			0.7		0.7	µs
t _{TLH}	LOW to HIGH output transition time	A port			3		3	ns
		B port			9		3	ns
t _{THL}	HIGH to LOW output transition time	A port			3		3	ns
		B port			3		3	ns
t _{sk(o)}	Output skew time	Between channels			0.3		0.3	ns
t _W	Pulse width	Data inputs		25		25		ns
f _{data}	Data rate	DDR	^[3] ^[4]	0.128	40	0.128	40	Mbit/s
V _{CCA} = 1.2 V ± 10 %								
t _{PHL}	HIGH to LOW propagation delay	A to B			5		5	ns
t _{PLH}	LOW to HIGH propagation delay	A to B			5		5	ns
t _{PHL}	HIGH to LOW propagation delay	B to A			5		4	ns
t _{PLH}	LOW to HIGH propagation delay	B to A			2		2	ns

4-bit Dual Supply Translating Transceiver; Auto Direction Sensing

Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for waveform see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions		V _{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
t _{en}	Enable time	OE to A; B			3		3	µs
t _{dis}	Disable time	OE to A; no external load	^[2]		0.4		0.4	µs
		OE to B; no external load	^[2]		0.4		0.4	µs
		OE to A			0.8		0.8	µs
		OE to B			0.7		0.7	µs
t _{TLH}	LOW to HIGH output transition time	A port			6		4	ns
		B port			6		3	ns
t _{THL}	HIGH to LOW output transition time	A port			3		3	ns
		B port			3		3	ns
t _{sk(o)}	Output skew time	Between channels			0.3		0.3	ns
t _W	Pulse width	Data inputs		25		25		ns
f _{data}	Data rate	DDR	^[3] ^[4]	0.128	40	0.128	40	Mbit/s
V _{CCA} = 1.8 V ± 10 %								
t _{PHL}	HIGH to LOW propagation delay	A to B			5		5	ns
t _{PLH}	LOW to HIGH propagation delay	A to B			5		5	ns
t _{PHL}	HIGH to LOW propagation delay	B to A			5		4	ns
t _{PLH}	LOW to HIGH propagation delay	B to A			3		3	ns
t _{en}	Enable time	OE to A; B			3		3	µs
t _{dis}	Disable time	OE to A; no external load	^[2]		0.4		0.4	µs
		OE to B; no external load	^[2]		0.4		0.4	µs
		OE to A			0.8		0.8	µs
		OE to B			0.7		0.7	µs

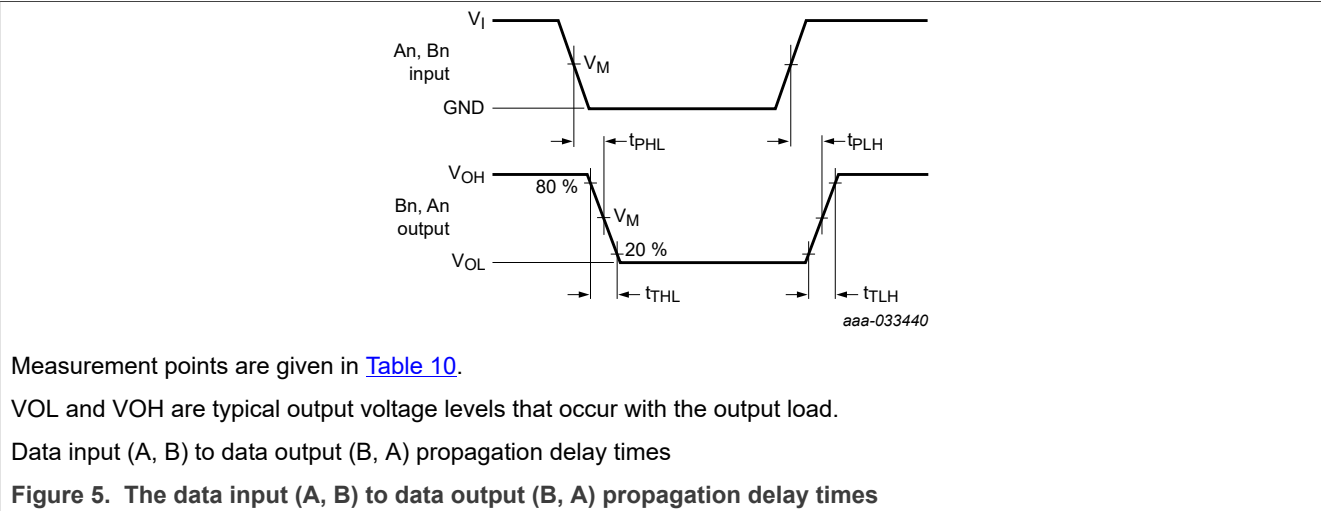
Table 9. Dynamic characteristics for temperature range -40 °C to +125 °C^[1]...continued
Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 7](#); for waveform see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions		V _{CCB}				Unit
				1.8 V ± 10 %		3.3 V ± 10 %		
				Min	Max	Min	Max	
t _{TLH}	LOW to HIGH output transition time	A port		6		4	ns	
		B port		6		3	ns	
t _{THL}	HIGH to LOW output transition time	A port		3		3	ns	
		B port		3		3	ns	
t _{sk(o)}	Output skew time			0.3		0.3	ns	
t _w	Pulse width	Data inputs		25		25	ns	
f _{data}	Data rate	DDR	^[3] ^[4]	0.128	40	0.128	40	Mbit/s

[1] t_{en} is the same as t_{pZL} and t_{pZH}; t_{dis} is the same as t_{pLZ} and t_{pHZ}.
[2] Delay between OE going LOW and when the outputs are disabled.
[3] Assuming CL (load capacitance) ≤ 50 pF and equal time for 1-bit and 0-bit information. The one-shot accelerator duration (30 ns max) is proportional to CL and determined by the internal circuit.
[4] The spec is DDR (Double data rate) per bit. The 40 Mbit/s equivalents to 20 MHz.

14 Waveforms

This section covers the waveform information, including test circuits and test data to support the information.



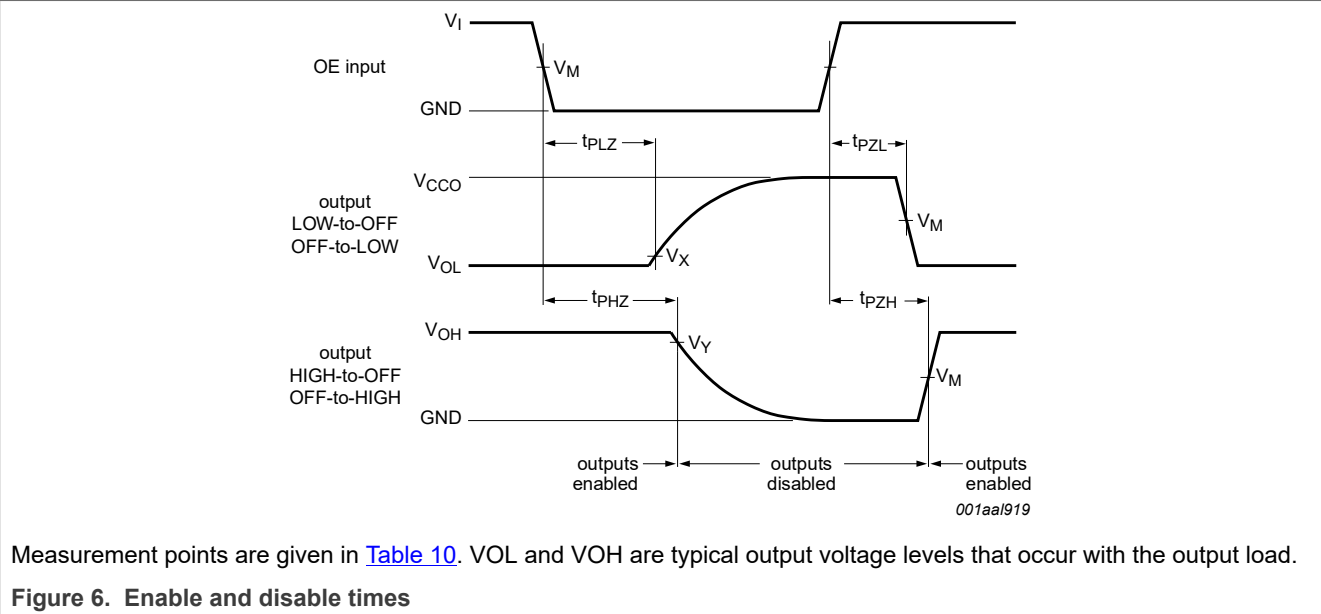


Table 10. Measurement points

V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

Supply Voltage	Input ^[1]	Output ^[2]		
V_{CCO}	V_M	V_M	V_X	V_Y
0.8 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.08 V	VOH - 0.08 V
1.2 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.12 V	VOH - 0.12 V
1.8 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.18 V	VOH - 0.18 V
3.3 V ± 10 %	0.4 V_{CCI}	0.4 V_{CCO}	VOL + 0.3 V	VOH - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.

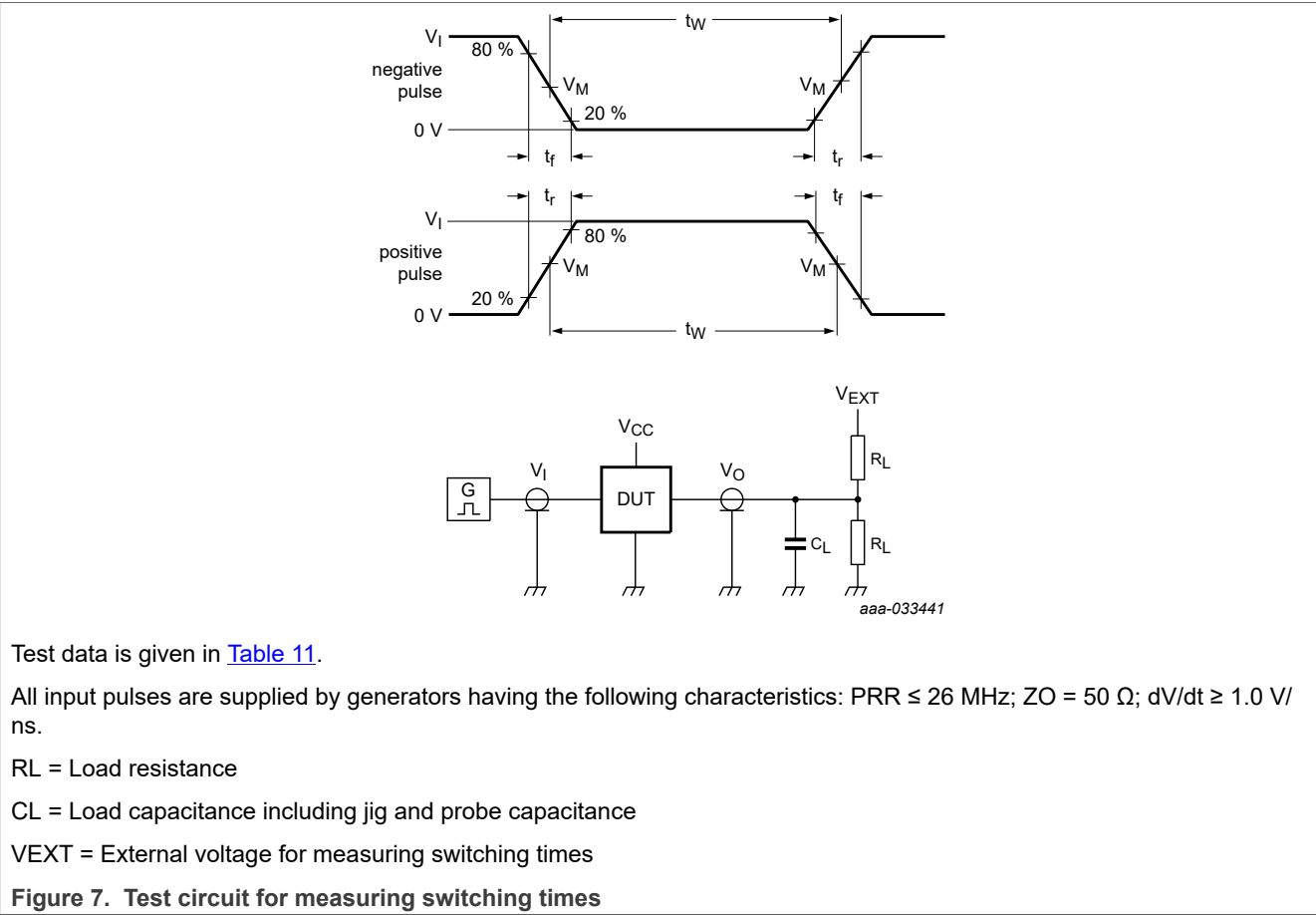


Table 11. Test data

Supply Voltage		Input		Load		V _{EXT}		
V _{CCA}	V _{CCB}	V _I ^[1]	Δt/ΔV	CL ^[2]	RL ^[3]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ} ^[4]
0.72 V to 1.98 V; & ≤ V _{CCB}	1.62 V to 3.63 V	V _{CCI}	≤ 1.0 ns/V	50 pF	50 kΩ, 1 MΩ	Open	Open	2 V _{CCO}

[1] V_{CCI} is the supply voltage associated with the input.

[2] For I3C maximum CL.

[3] For measuring data rate, pulse width, propagation delay, and output rise and fall measurements, RL = 1 MΩ; for measuring enable and disable times, RL = 50 kΩ.

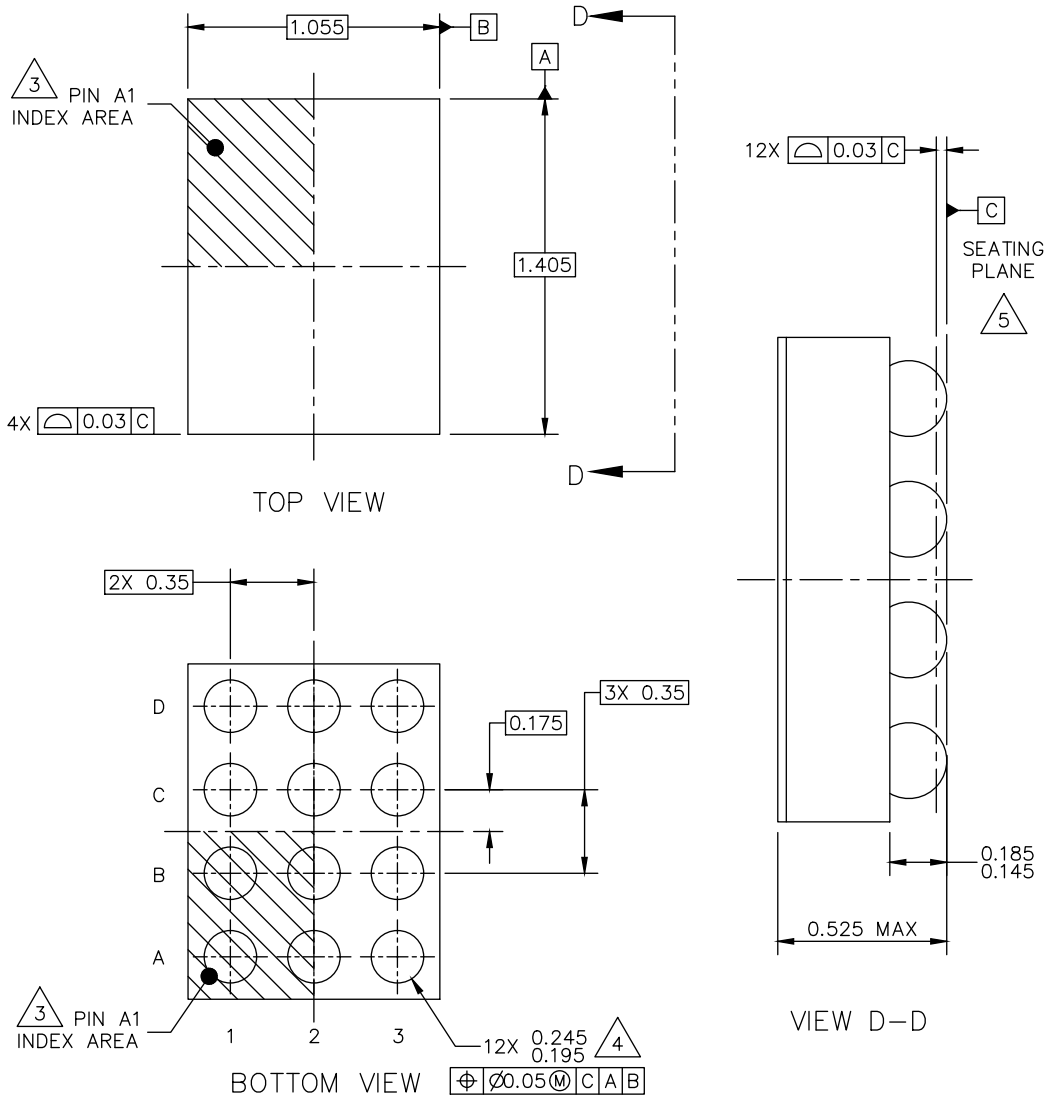
[4] V_{CCO} is the supply voltage associated with the output.

15 Package outline

This section covers the package outline for SOT2063-4 (WLCSP12) and the notes associated with it.

WLCSP-12 I/O
1.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4



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Figure 8. Package outline SOT2063-4 (WLCSP12)

WLCSP-12 I/O
.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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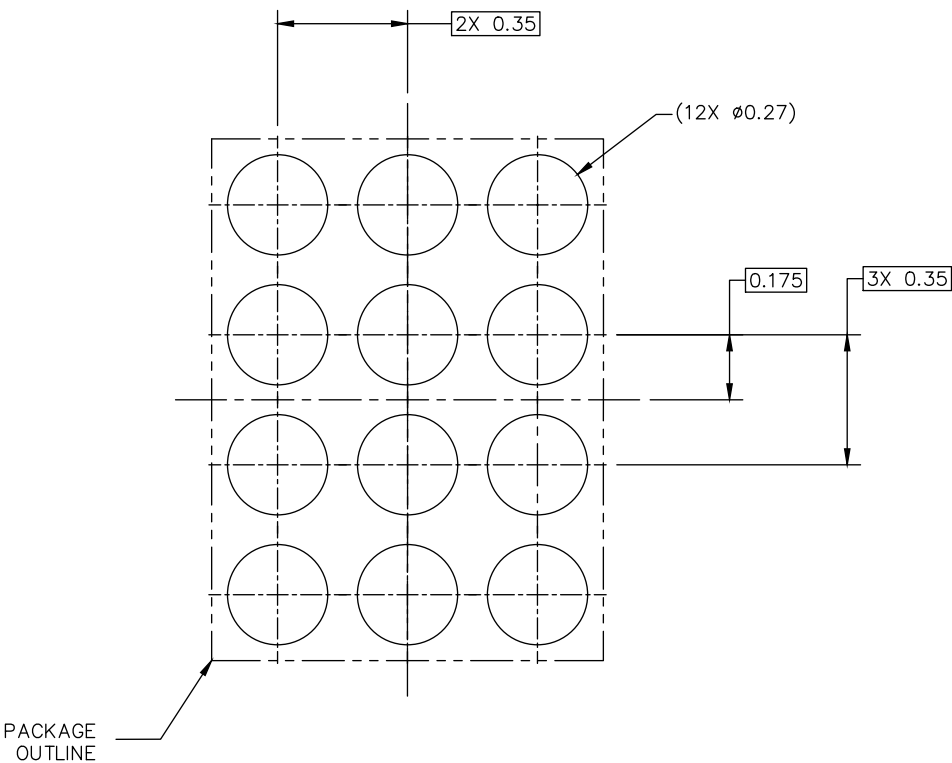
Figure 9. Package outline SOT2063-4 (WLCSP12); notes

16 Soldering

This section provides the figures of footprints for soldering operation.

WLCSP-12 I/O
1.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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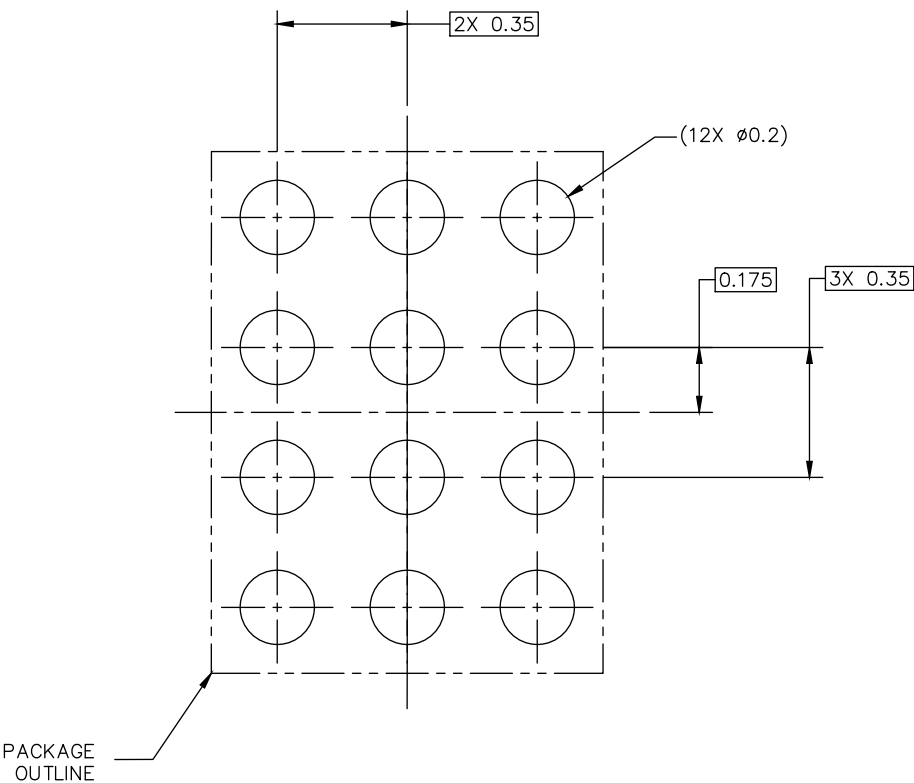
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Figure 10. Soldering footprint for SOT2063-4 (WLCSP12); solder mask opening pattern

WLCSP-12 I/O
1.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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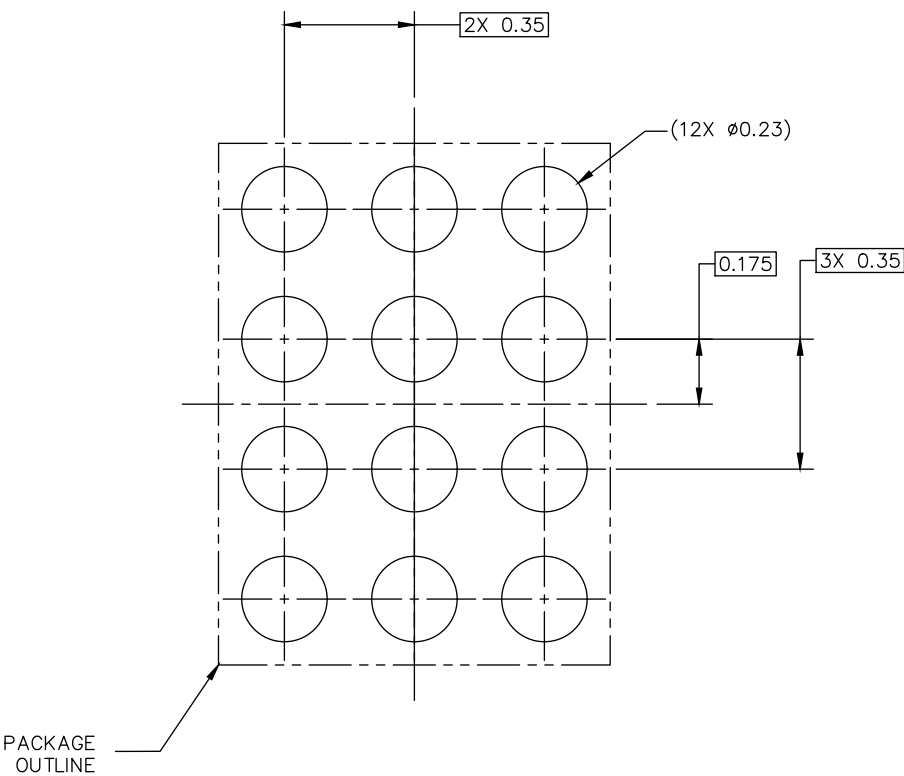
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Figure 11. Soldering footprint for SOT2063-4 (WLCSP12); I/O pads and solderable area

WLCSP-12 I/O
.405 X 1.055 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2063-4



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 12. Soldering footprint for SOT2063-4 (WLCSP12); solder paste stencil

17 Revision history

Table 12. Revision history

Document ID	Release date	Description
P3A1604UK v.1.1	27 June 2025	<ul style="list-style-type: none">Updated per CIN# 202506029I<ul style="list-style-type: none">Updated Figure 1Editorial fixes
P3A1604UK v.1.0	10 December 2024	<ul style="list-style-type: none">Initial version

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1 General description 2

2 Features and benefits 2

3 Applications 2

4 Ordering information 2

4.1 Ordering options 3

5 Block diagram 3

6 Pinning information 4

6.1 Pinning 4

6.2 Pin description 4

7 Functional description 4

7.1 Architecture 5

7.2 Input driver requirements 5

7.3 Output load considerations 5

7.4 Power up 5

7.5 Enable and disable 6

7.6 Pull-up or pull-down resistors on I/O lines 6

8 Application information 6

8.1 Applications 6

8.2 Architecture 7

9 Limiting values 8

10 Thermal characteristics 9

11 Recommended operating conditions 9

12 Static characteristics 9

13 Dynamic characteristics 11

14 Waveforms 14

15 Package outline 16

16 Soldering 18

17 Revision history 22

Legal information 23

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