MAX14938/MAX14939

2.75kV$_{RMS}$ Isolated 20Mbps Half-Duplex PROFIBUS/RS-485 Transceivers with ±35kV ESD Protection

General Description

The MAX14938/MAX14939 isolated RS-485/PROFIBUS-DP transceivers provide 2750V$_{RMS}$ (60s) of galvanic isolation between the cable side (RS-485 driver/receiver side) and the UART side of the device. Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. These devices allow for robust communication up to 20Mbps.

An integrated LDO provides a simple and space-efficient architecture for providing power to the cable side of the IC.

Each device includes one half-duplex driver/receiver channel. The receiver is 1/4-unit load, allowing up to 128 transceivers on a common bus.

Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when cable-side or UART-side power supplies are below functional levels.

The driver outputs/receiver inputs are protected from ±35kV electrostatic discharge (ESD) to GNDB on the cable side, as specified by the Human Body Model (HBM).

The MAX14938/MAX14939 are available in a wide-body 16-pin SOIC package and operate over the -40°C to +105°C temperature range.

Functional Diagram

() MAX14938 only
* MAX14939 only
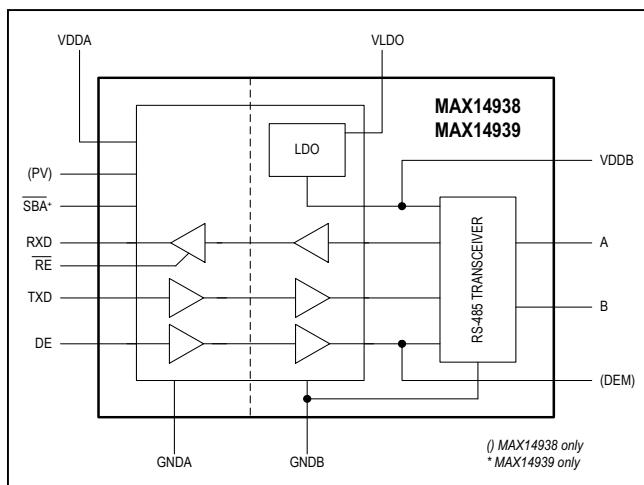
Benefits and Features

- High-Performance Transceiver Enables Flexible Designs
  - Integrated LDO for Cable-Side Power
  - Compliant with RS-485 EIA/TIa-485 Standard
  - 20Mbps Maximum Data Rate
  - Allows Up to 128 Devices on the Bus
- Integrated Protections Ensures Robust Communication
  - ±35kV ESD (HBM) on Driver Outputs/Receiver Inputs
  - 2.75kV$_{RMS}$ Withstand Isolation Voltage for 60s (V$_{ISO}$)
  - 630V$_{PEAK}$ Maximum Repetitive Peak-Isolation Voltage (V$_{IORM}$)
  - 445V$_{RMS}$ Maximum Working-Isolation Voltage (V$_{IOWM}$)
  - > 30 Years Lifetime at Rated Working Voltage
  - Withstands ±10kV Surge per IEC 61000-4-5
  - Thermal Shutdown

Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A

Applications

- Industrial Automation Equipment
- Programmable Logic Controllers
- HVAC
- Power Meters

Ordering Information appears at end of data sheet.

maxim integrated™

Absolute Maximum Ratings

V$_{DDA}$ to GNDA ....-0.3V to +6V
V$_{DDB}$ to GNDB...-0.3V to +6V
V$_{LDO}$ to GNDB ....-0.3V to +16V
TXD, DE, $\overline{RE}$, PV to GNDA ....-0.3V to +6V
$\overline{SBA}$, RXD to GNDA ....-0.3V to (V$_{DDA}$ + 0.3V)
DEM to GNDB ....-0.3V to (V$_{DDB}$ + 0.3V)
A, B to GNDB..-8V to +13V
Short Circuit Duration (RXD, $\overline{SBA}$ to GNDA,
   A, B, DEM ,V$_{DDB}$ to GNDB).................................Continuous

Continuous Power Dissipation (T$_A$ = +70°C)
   16-pin W SOIC (derate 14.1mW/°C
   above +70°C) 1126.8mW
Operating Temperature Range........................ -40°C to +105°C
Junction Temperature...+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).....................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ$_{JA}$) ....71°C/W

Junction-to-Case Thermal Resistance (θ$_{JC}$)..................23°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

(V$_{DDA}$ − V$_{GNDA}$ = 1.71V to 5.5V, V$_{DDB}$ − V$_{GNDB}$ = 4.5V to 5.5V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at V$_{DDA}$ − V$_{GNDA}$ = 3.3V, V$_{DDB}$ − V$_{GNDB}$ = 5V, V$_{GNDA}$ = V$_{GNDB}$, and T$_A$ = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V$_{DDA}$		1.71		5.5	V
	V$_{DDB}$		4.5		5.5	
Supply Current	I$_{DDA}$	V$_{DDA}$ = 5V, DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no load		4	6.6	mA
	I$_{DDB}$	DE = high, $\overline{RE}$ = TXD = low, RXD unconnected, no bus load, V$_{DDB}$ = 5V		7.6	12.5	
Undervoltage-Lockout Threshold	V$_{UVLOA}$	V$_{DDA}$ rising	1.50	1.58	1.65	V
	V$_{UVLOB}$	V$_{DDB}$ rising	2.55	2.7	2.85	
Undervoltage-Lockout Threshold Hysteresis	V$_{UVHYSTA}$			50		mV
	V$_{UVHYSTB}$			200		
LDO						
LDO Supply Voltage	V$_{LDO}$	Relative to GNDB, LDO is on (Note 4)	4.68		14	V
LDO Supply Current	I$_{LDO}$	DE = high, TXD = low, no bus load, V$_{LDO}$ = 5V		7.7	12.9	mA
LDO Output Voltage	V$_{DDB}$		4.5	5	5.5	V
LDO Current Limit				300		mA
Load Regulation		V$_{LDO}$ = 5.68V, I$_{LOAD}$ = 20mA to 40mA		0.19	1.7	mV/mA
Line Regulation		V$_{LDO}$ = 5.68V to 14V, I$_{LOAD}$ = 20mA		0.12	4.5	mV/V

DC Electrical Characteristics (continued)

(V$_{DDA}$ − V$_{GNDA}$ = 1.71V to 5.5V, V$_{DDB}$ − V$_{GNDB}$ = 4.5V to 5.5V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at V$_{DDA}$ − V$_{GNDA}$ = 3.3V, V$_{DDB}$ − V$_{GNDB}$ = 5V, V$_{GNDA}$ = V$_{GNDB}$, and T$_A$ = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage		V$_{LDO}$ = 4.68V, I$_{DDB}$ = 120mA			100	180	mV
Load Capacitance		Nominal value (Note 8)		1		10	µF
LOGIC INTERFACE (TXD, RXD, DE, $\overline{RE}$, $\overline{SBA}$, PV, DEM)							
Input High Voltage	V$_{IH}$	$\overline{RE}$, TXD, DE, PV to GNDA	2.25V < V$_{DDA}$ < 5.5V	0.7 x V$_{DDA}$			V
			1.71V < V$_{DDA}$ < 1.89V	0.78 x V$_{DDA}$			
Input Low Voltage	V$_{IL}$	$\overline{RE}$, TXD, DE, PV to GNDA	2.25V < V$_{DDA}$ < 5.5V			0.8	V
			1.71V < V$_{DDA}$ < 1.89V			0.6	
Input Hysteresis	V$_{HYS}$	$\overline{RE}$, TXD, DE, PV to GNDA			220		mV
Input Capacitance	C$_{IN}$	$\overline{RE}$, TXD, DE, PV, f$_{SW}$ = 1MHz			2		pF
Input Pull-Up Current	I$_{PU}$	TXD, PV		-10	-4.5	-1.5	µA
Input Pull-Down Current	I$_{PD}$	DE, $\overline{RE}$		1.5	4.5	10	µA
$\overline{SBA}$ Pull-Up Resistance	R$_{SBA}$	MAX14939 only		3	5	8	kΩ
Output Voltage High	V$_{OH}$	RXD to GNDA, I$_{OUT}$ = -4mA		V$_{DDA}$ -0.4			V
		MAX14938 only, DEM to GNDB, I$_{OUT}$ = -4mA		V$_{DDB}$ -0.4			
Output Voltage Low	V$_{OL}$	RXD to GNDA, I$_{OUT}$ = 4mA				0.40	V
		MAX14938 only, DEM to GNDB, I$_{OUT}$ = 4mA				0.40	
		MAX14939 only, $\overline{SBA}$ to GNDA, I$_{OUT}$ = 4mA				0.45	
Short-Circuit Output Pullup Current	I$_{SH\_PU}$	0V ≤ V$_{RXD}$ ≤ V$_{DDA}$, $\overline{RE}$ = low		-42			mA
		MAX14938 only, 0V ≤ V$_{DEM}$ ≤ V$_{DDB}$, DE = high, PV = high		-42			
Short-Circuit Output Pulldown Current	I$_{SH\_PD}$	0V ≤ V$_{RXD}$ ≤ V$_{DDA}$, $\overline{RE}$ = low				+40	mA
		MAX14938 only, 0V ≤ V$_{DEM}$ ≤ V$_{DDB}$, DE = low, PV = high				+40	
		MAX14939 only, 0V ≤ V$_{\overline{SBA}}$ ≤ V$_{DDA}$, side B is powered and working				+60	
Three-State Output Current	I$_{OZ}$	0V ≤ V$_{RXD}$ ≤ V$_{DDA}$, $\overline{RE}$ = high		-1		+1	µA

DC Electrical Characteristics (continued)

(V_{DDA} − V_{GNDA} = 1.71V to 5.5V, V_{DDB} − V_{GNDB} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DDA} − V_{GNDA} = 3.3V, V_{DDB} − V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output	|V$_{OD}$|	R_L = 54Ω, TXD = high or low, Figure 1a		2.1			V
		R_L = 100Ω, TXD = high or low, Figure 1a		2.9			
		-7V ≤ V_{CM} ≤ +12V, Figure 1b		1.5		5	
Differential Driver Peak-to-Peak Output	V$_{ODPP}$	Figure 2 (Note 5)		4.0		6.8	V
Change in Magnitude of Differential Driver Output Voltage	ΔV$_{OD}$	R_L = 54Ω (Note 6)		-0.2		+0.2	V
Driver Common Mode Output Voltage	V$_{OC}$	R_L = 54Ω, Figure 1a			1.8	3	V
Change in Magnitude of Common-Mode Voltage	ΔV$_{OC}$	R_L = 54Ω, Figure 1a (Note 6)		-0.2		+0.2	V
Driver Short-Circuit Output Current	I$_{OSD}$	GNDB ≤ V_{OUT} ≤ +12V, output low (Note 7)				+250	mA
		-7V ≤ V_{OUT} ≤ V_{DDB}, output high (Note 7)		-250			
Driver Short-Circuit Foldback Output Current	I$_{OSDF}$	(V_{DDB} − 1V) ≤ V_{OUT} ≤ +12V, output low (Note 7, 8)		+15			mA
		-7V ≤ V_{OUT} ≤ +1V, output high (Note 7, 8)				-15	
RECEIVER							
Input Current (A and B)	I$_A$, I$_B$	DE = low, V_{DDB} = GNDB or 5.5V	V$_{IN}$ = +12V			+250	µA
			V$_{IN}$ = -7V	-200			
Receiver Differential Threshold Voltage	V$_{TH}$	-7V ≤ V_{CM} ≤ +12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV$_{TH}$	V_{CM} = 0V			15		mV
Receiver Input Resistance	R$_{IN}$	-7V ≤ V_{CM} ≤ +12V, DE = low		48			kΩ
Differential Input Capacitance	C$_{A,B}$	Measured between A and B, DE = $\overline{RE}$ = low at 6MHz			8		pF

DC Electrical Characteristics (continued)

($V_{DDA} - V_{GNDA}$ = 1.71V to 5.5V, $V_{DDB} - V_{GNDB}$ = 4.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA}$ = 3.3V, $V_{DDB} - V_{GNDB}$ = 5V, $V_{GNDA} = V_{GNDB}$, and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION						
Thermal-Shutdown Threshold	T_{SHDN}	Temperature Rising		+160		°C
Thermal-Shutdown Hysteresis	T_{HYST}			15		°C
ESD Protection (A and B Pins to GNDB)		Human Body Model		±35		kV
		IEC 61000-4-2 Air Gap Discharge		±12		
		IEC 61000-4-2 Contact Discharge		±10		
ESD Protection (All Other Pins)		Human Body Model		±4		kV

Switching Electrical Characteristics

($V_{DDA} - V_{GNDA}$ = 1.71V to 5.5V, $V_{DDB} - V_{GNDB}$ = 4.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA}$ = 3.3V, $V_{DDB} - V_{GNDB}$ = 5V, $V_{GNDA} = V_{GNDB}$, and T_A = +25°C.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
Common Mode Transient Immunity	CMTI	(Note 9)		35		kV/µs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
DRIVER						
Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF, Figure 3 and Figure 4			68	ns
Differential Driver Output Skew $\lvert t_{DPLH} - t_{DPHL} \rvert$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF, Figure 3 and Figure 4			6	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF, Figure 3 and Figure 4			15	ns
Maximum Data Rate	DR_{MAX}		20			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, C_L = 50pF, Figure 5			88	ns

Switching Electrical Characteristics (continued)

(V$_{DDA}$ − V$_{GNDA}$ = 1.71V to 5.5V, V$_{DDB}$ − V$_{GNDB}$ = 4.5V to 5.5V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at V$_{DDA}$ − V$_{GNDA}$ = 3.3V, V$_{DDB}$ − V$_{GNDB}$ = 5V, V$_{GNDA}$ = V$_{GNDB}$, and T$_A$ = +25°C.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable to Output Low	t$_{DZL}$	R$_L$ = 500Ω, C$_L$ = 50pF, Figure 6			88	ns
Driver Disable Time from Low	t$_{DLZ}$	R$_L$ = 500Ω, C$_L$ = 50pF, Figure 6			80	ns
Driver Disable Time from High	t$_{DHZ}$	R$_L$ = 500Ω, C$_L$ = 50pF, Figure 5			80	ns
RECEIVER						
Receiver Propagation Delay	t$_{RPLH}$, t$_{RPHL}$	C$_L$ = 15pF, Figure 7 and 8 (Note 10)			68	ns
Receiver Output Skew |t$_{RPLH}$ - t$_{RPHL}$|	t$_{RSKEW}$	C$_L$ = 15pF, Figure 7 and 8 (Note 10)			6	ns
Maximum Data Rate	DR$_{MAX}$		20			Mbps
Receiver Enable to Output High	t$_{RZH}$	R$_L$ = 1kΩ, C$_L$ = 15pF, S2 closed, Figure 9			20	ns
Receiver Enable to Output Low	t$_{RZL}$	R$_L$ = 1kΩ, C$_L$ = 15pF, S1 closed, Figure 9			30	ns
Receiver Disable Time From Low	t$_{RLZ}$	R$_L$ = 1kΩ, C$_L$ = 15pF, S1 closed, Figure 9			20	ns
Receiver Disable Time From High	t$_{RHZ}$	R$_L$ = 1kΩ, C$_L$ = 15pF, S2 closed, Figure 9			20	ns

Note 2: All devices are 100% production tested at T$_A$ = +25°C. Specifications over temperature are guaranteed by design.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: V$_{LDO}$ max indicates voltage capability of the circuit. Power dissipation requirements may limit V$_{LDO}$ max to a lower value.

Note 5: V$_{ODPP}$ is the difference in V$_{OD}$ when TXD is high and when TXD is low.

Note 6: ΔV$_{OD}$ and ΔV$_{OC}$ are the changes in V$_{OD}$ and V$_{OC}$, respectively, when the TXD input changes state.

Note 7: The short circuit output current applies to the peak current just prior to foldback current limiting.

Note 8: Not production tested. Guaranteed by design.

Note 9: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB. ΔV$_{CM}$ = 1kV.

Note 10: Capacitive load includes test probe and fixture capacitance.

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V$_{PR}$	Method B1 = V$_{IORM}$ x 1.875 (t = 1s, partial discharge < 5pC)	1182	V$_P$
Maximum Repetitive Peak Withstand Voltage	V$_{IORM}$	(Note 11)	630	V$_P$
Maximum Working Isolation Voltage	V$_{IOWM}$	(Note 11)	445	V$_{RMS}$
Maximum Transient Isolation Voltage	V$_{IOTM}$	t = 1s	4600	V$_P$
Maximum Withstand Isolation Voltage	V$_{ISO}$	t = 60s, f = 60Hz (Note 11, 12)	2750	V$_{RMS}$
Maximum surge Isolation Voltage	V$_{IOSM}$	IEC 61000-4-5, 1.2/50µs	10	kV
Insulation Resistance	R$_S$	T$_A$ = +150°C, V$_{IO}$ = 500V	>10^9	Ω
Barrier Capacitance Input to Output	CIO		2	pF
Creepage Distance	CPG	Wide SO	8	mm
Clearance Distance	CLR	Wide SO	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparitive Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 11: V$_{IORM}$, V$_{IOWM}$, and V$_{ISO}$ are defined by the IEC 60747-5-5 standard.
Note 12: Product is qualified at V$_{ISO}$ for 60 seconds. 100% production tested at 120% of V$_{ISO}$ for 1 second.

Safety Regulatory Approvals

UL
The MAX14938/MAX14939 is certified under UL1577. For more details, see File E351759.
Rate up to 2750VRMS isolation voltage for basic insulation.
cUL
The MAX14938/MAX14939 is certified under UL1577. For more details, see File E351759. Rate up to 2750V$_{RMS}$ isolation voltage for basic insulation.
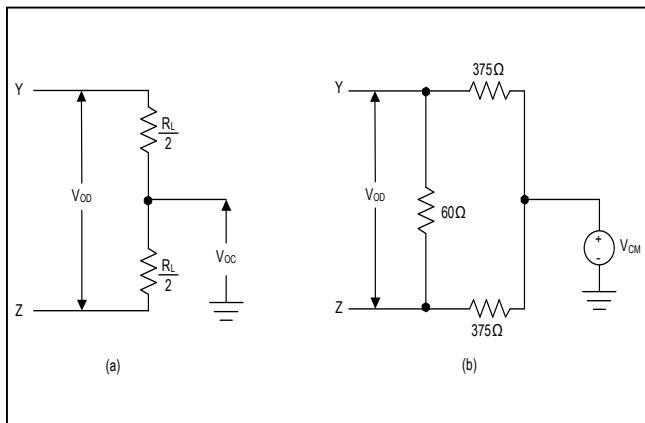
Figure 1. Driver DC Test Load
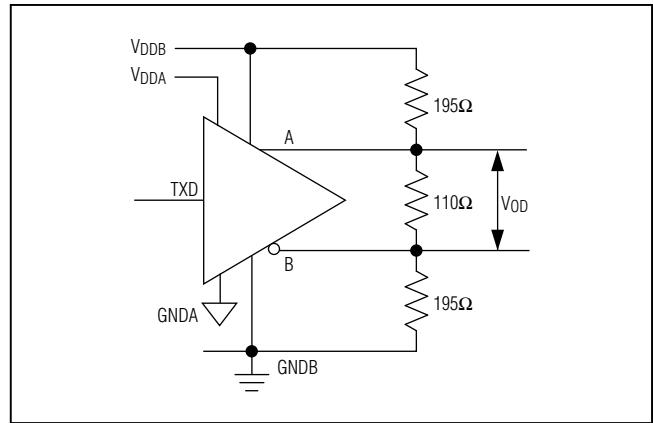
Figure 2. V$_{ODPP}$ Swing Under PROFIBUS Equivalent Load Test
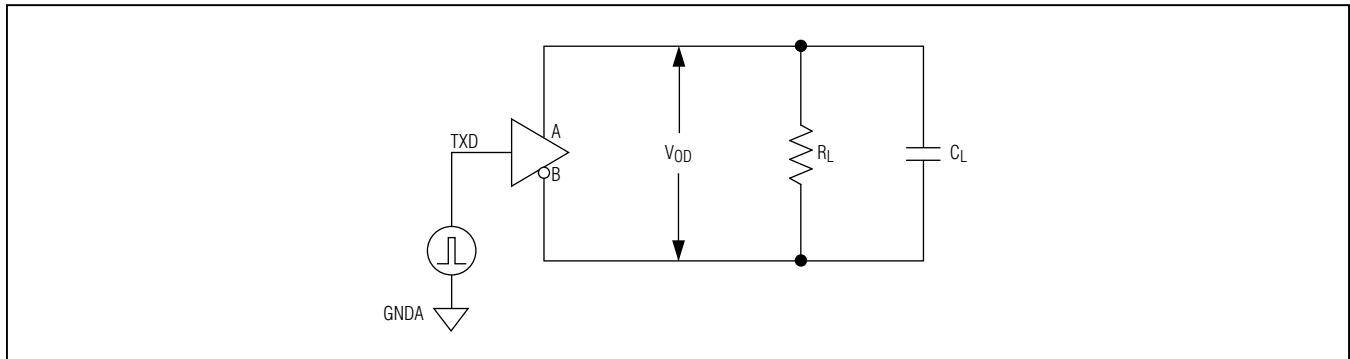
Figure 3. Driver Timing Test Circuit
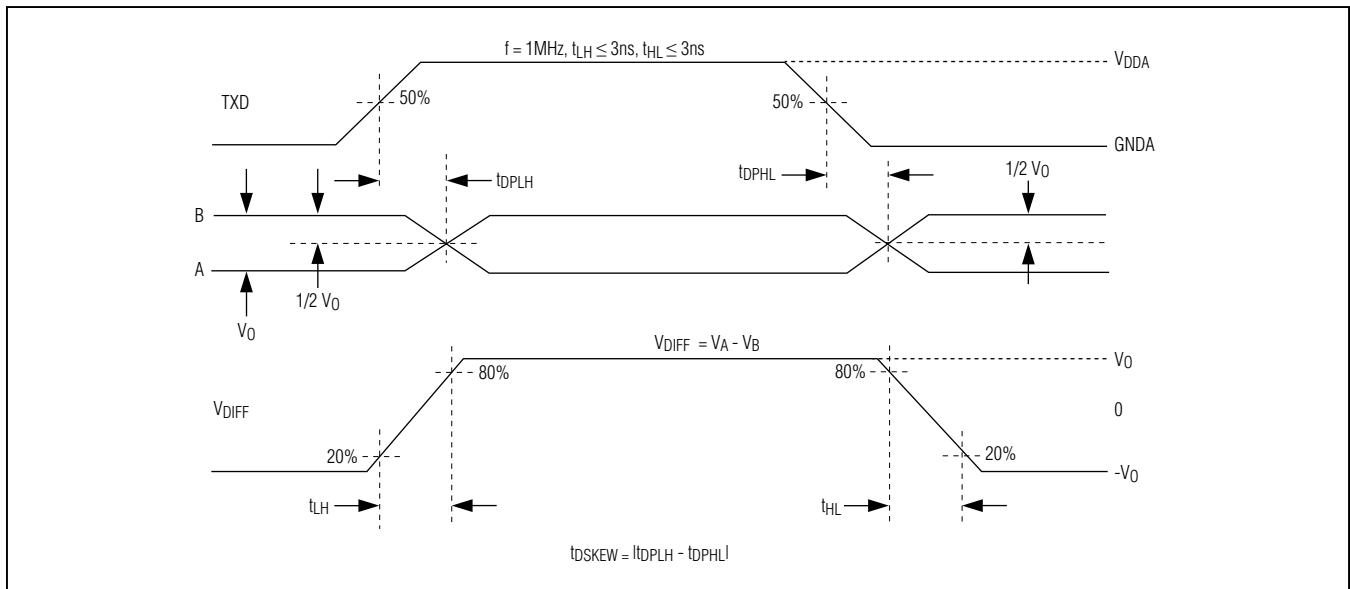
Figure 4. Driver Propagation Delays
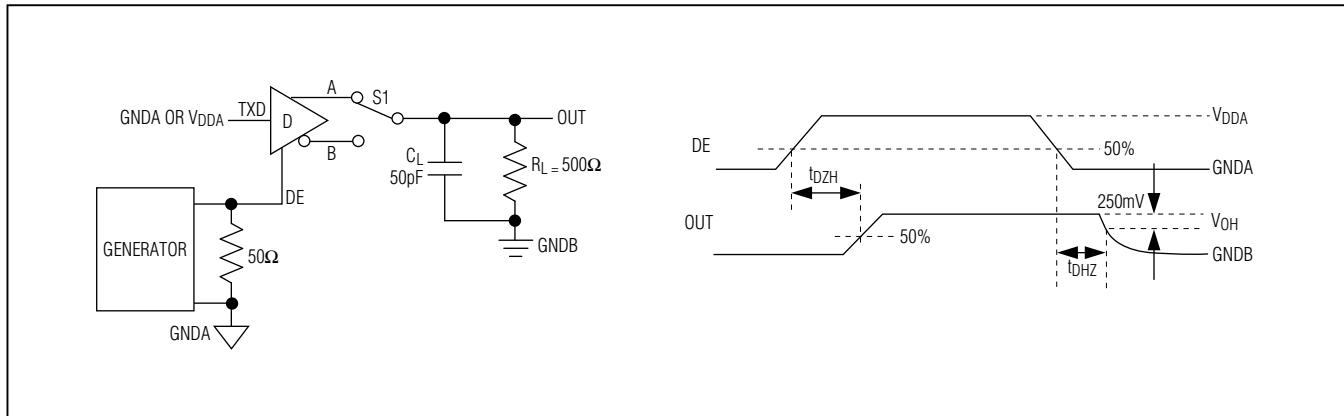
Figure 5. Driver Enable and Disable Times (t$_{DHZ}$, t$_{DZH}$)

Figure 6. Driver Enable and Disable Times (t$_{DZL}$, t$_{DLZ}$)
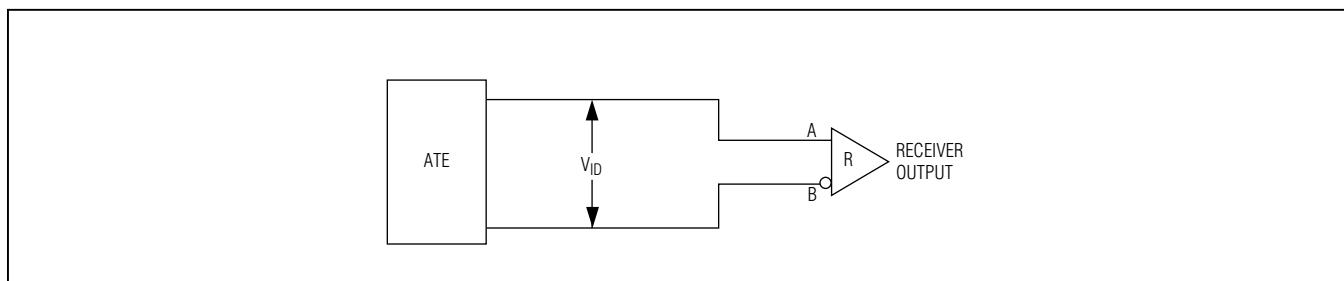
Figure 7. Receiver Propagation Delay Test Circuit
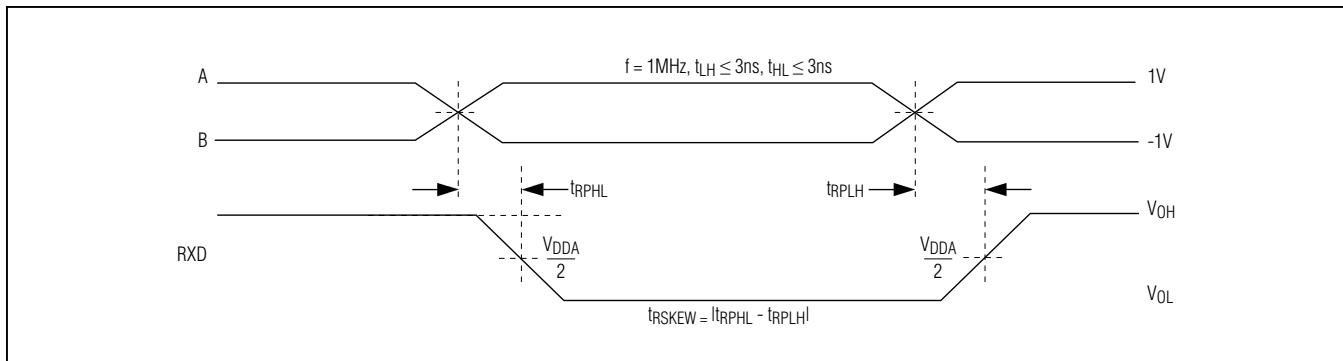
Figure 8. Receiver Propagation Delays
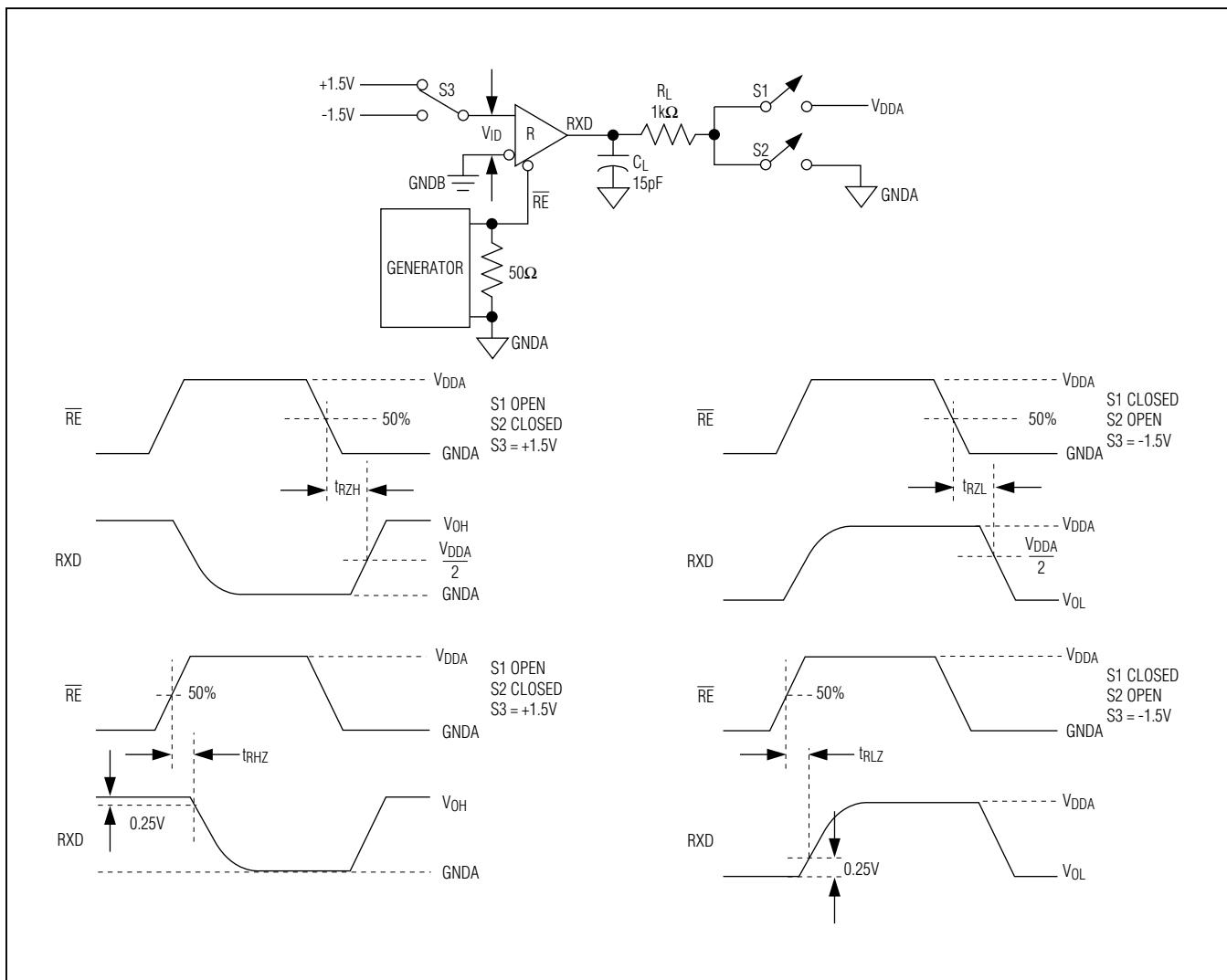
Figure 9. Receiver Enable and Disable Times

Typical Operating Characteristics

($V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 5V$, $V_{GNDA} = V_{GNDB}$, and $T_A = +25°C$, unless otherwise noted.)
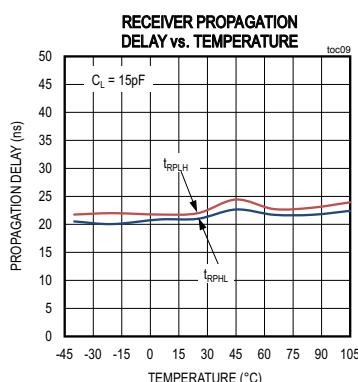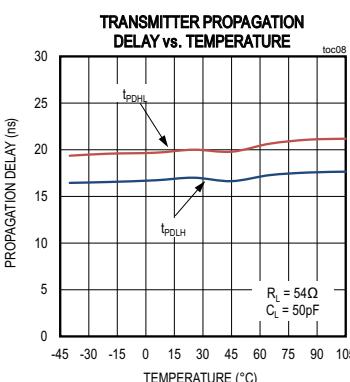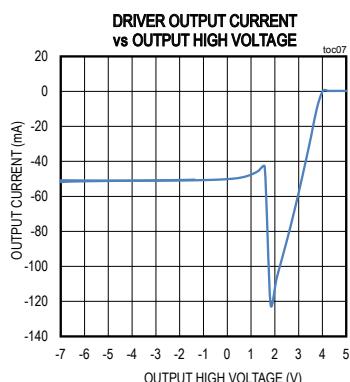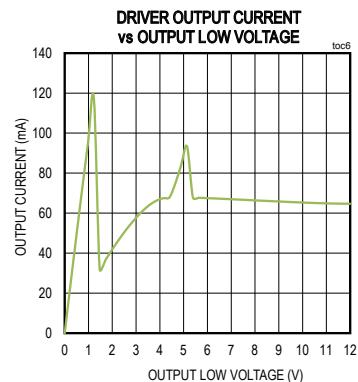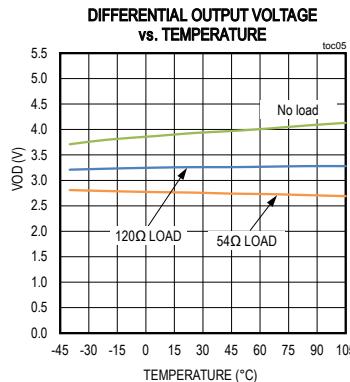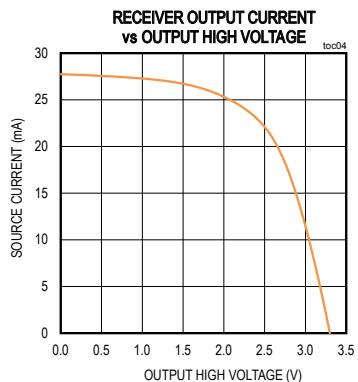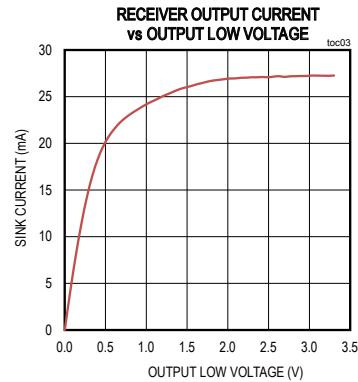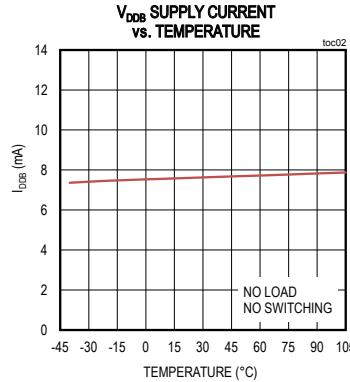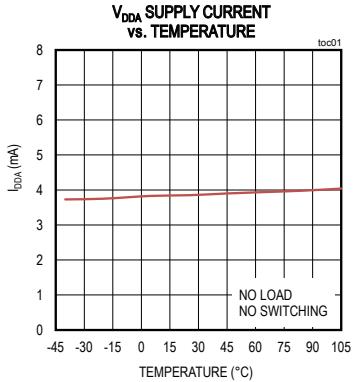
Typical Operating Characteristics (continued)

(V_{DDA} − V_{GNDA} = 3.3V, V_{DDB} − V_{GNDB} = 5V, V_{GNDA} = V_{GNDB}, and T_A = +25°C, unless otherwise noted.)

DRIVER ENABLE/DISABLE
DELAY vs. TEMPERATURE

DRIVER
PROPAGATION DELAY

RECEIVER
PROPAGATION DELAY

V_{DDA} SUPPLY CURRENT
vs. DATA RATE

V_{DDB} SUPPLY
CURRENT vs. DATA RATE

Pin Configuration

TOP VIEW

MAX14938	
VDDA 1	16 VDDB
GNDA 2	15 GNDB
RXD 3	14 N.C.
$\overline{RE}$ 4	13 B
DE 5	12 A
TXD 6	11 VLDO
PV 7	10 DEM
GNDA 8	9 GNDB

MAX14939	
VDDA 1	16 VDDB
GNDA 2	15 GNDB
RXD 3	14 N.C.
$\overline{RE}$ 4	13 B
DE 5	12 A
TXD 6	11 VLDO
$\overline{SBA}$ 7	10 N.C.
GNDA 8	9 GNDB

WIDE SOIC
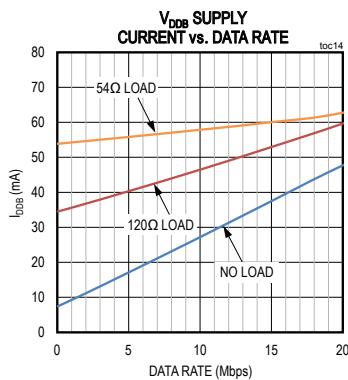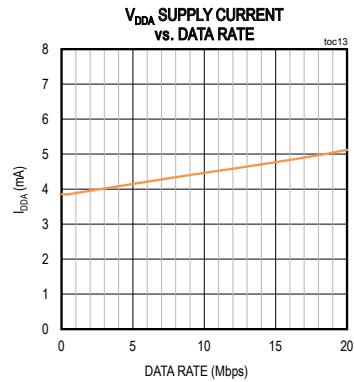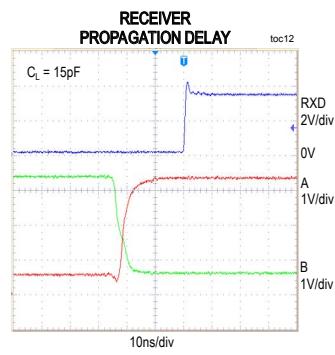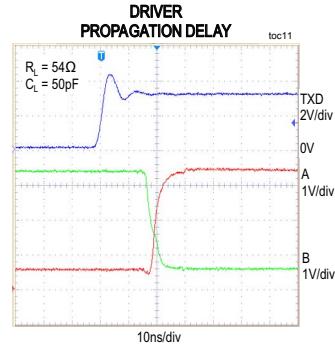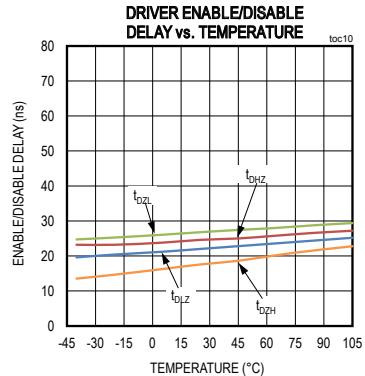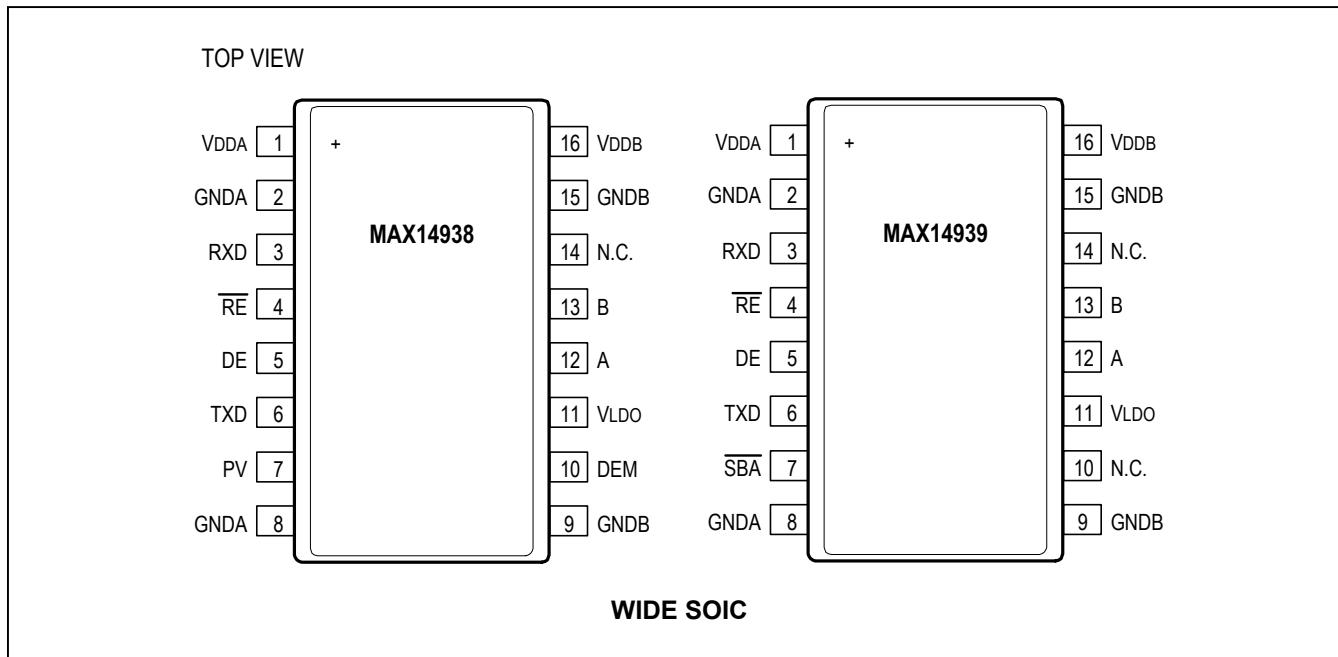
Pin Description

PIN		NAME	REFERENCE	FUNCTION
MAX14938	MAX14939			
1	1	V$_{DDA}$	GNDA	UART/Logic-Side Power Input. Bypass V$_{DDA}$ to GNDA with both 0.1µF and 1µF capacitors as close to the device as possible.
2, 8	2, 8	GNDA	-	UART/Logic-Side Ground. GNDA is the ground reference for digital signals.
3	3	RXD	GNDA	Receiver Data Output. Drive $\overline{RE}$ low to enable RXD. With $\overline{RE}$ low, RXD is high when $(V_A - V_B) > -50mV$ and is low when $(V_A - V_B) < -200mV$. RXD is high when V$_{DDB}$ is less than V$_{UVLOB}$. RXD is high impedance when $\overline{RE}$ is high.
4	4	$\overline{RE}$	GNDA	Receiver Output Enable. Driver $\overline{RE}$ low or connect to GNDA to enable RXD. Drive $\overline{RE}$ high to disable RXD. RXD is high-impedance when $\overline{RE}$ is high. $\overline{RE}$ has an internal 4.5µA pull-down to GNDA.
5	5	DE	GNDA	Driver Output Enable. Drive DE high to enable bus driver outputs A and B. Drive DE low or connect to GNDA to disable A and B. A and B are high impedance when DE is low. DE has an internal 4.5µA pull-down to GNDA.
6	6	TXD	GNDA	Driver Input. With DE high, a low on TXD forces the noninverting output (A) low and the inverting output (B) high. Similarly, a high on TXD forces the noninverting output high and the inverting output low. TXD has an internal 4.5µA pull-up to V$_{DDA}$.

Pin Description (continued)

PIN		NAME	REFERENCE	FUNCTION
MAX14938	MAX14939			
7	-	PV	GNDA	Power Valid Input. Hold PV low to disable the driver while the supplies stabilize. Pull PV high when power is stable to enable the driver. PV has an internal 4.5µA pull-up to V$_{DDA}$.
—	7	$\overline{SBA}$	GNDA	Side B Active Indicator Output. $\overline{SBA}$ asserts low when side B is powered and working. $\overline{SBA}$ has an internal 5kΩ pull-up resistor to V$_{DDA}$.
9, 15	9, 15	GNDB	—	Cable-Side Ground. GNDB is the ground reference for the internal LDO, the DEM output, and the Profibus/RS-485 bus signals.
10	-	DEM	GNDB	Driver Enable Monitor Output. DEM is high when the transmitter is enabled. See the Function Tables for more information.
14	10, 14	N.C.	—	No Connection. Not internally connected.
11	11	V$_{LDO}$	GNDB	LDO Power Input. Connect a minimum voltage of 4.68V to V$_{LDO}$ to power the cable-side of the transceiver. Bypass V$_{LDO}$ to GNDB with both 0.1µF and 1µF capacitors as close to the device as possible. To disable the internal LDO, leave V$_{LDO}$ unconnected or connect to GNDB.
12	12	A	GNDB	Noninverting Receiver Input and Noninverting Driver Output
13	13	B	GNDB	Inverting Receiver Input and Inverting Driver Output
16	16	V$_{DDB}$	GNDB	Cable-Side Power Input/Isolated LDO Power Output. Bypass V$_{DDB}$ to GNDB with both 0.1µF and 1µF capacitor as close to the device as possible. V$_{DDB}$ is the output of the internal LDO when power is applied to V$_{LDO}$. When the internal LDO is not used (V$_{LDO}$ is unconnected or connected to GNDB), V$_{DDB}$ is the positive supply input for the cable-side of the IC.

Function Tables

TRANSMITTING								
INPUTS					OUTPUTS			
V$_{DDA}$	V$_{DDB}$	DE	TXD	PV**	A	B	DEM**	
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	1	1	1	1	0	1	
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	1	0	1	0	1	1	
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	0	X	X	High-Z	High-Z	0	
< V$_{UVLOA}$	≥ V$_{UVLOB}$	X	X	X	High-Z	High-Z	0	
≥ V$_{UVLOA}$	< V$_{UVLOB}$	X	X	X	High-Z	High-Z	0	
< V$_{UVLOA}$	< V$_{UVLOB}$	X	X	X	High-Z	High-Z	0	

Note: Drive DE low to disable the transmitter outputs. Drive DE high to enable the transmitter outputs. DE has an internal pull-down to GNDA.

** MAX14938 only, X = Don't care

RECEIVING				
INPUTS				OUTPUTS
V$_{DDA}$	V$_{DDB}$	$\overline{RE}$	(V$_A$- V$_B$)	RXD
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	0	> -50mV	1
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	0	< -200mV	0
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	0	Open/Short	1
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	1	X	High-Z
< V$_{UVLOA}$	≥ V$_{UVLOB}$	X	X	High-Z
≥ V$_{UVLOA}$	< V$_{UVLOB}$	0	X	1
< V$_{UVLOA}$	< V$_{UVLOB}$	X	X	High-Z

Note: Drive $\overline{RE}$ high to disable the receiver output. Drive $\overline{RE}$ low to enable to receiver output. $\overline{RE}$ has an internal pulldown to GNDA.

X = Don't care

$\overline{SBA}$		
V$_{DDA}$	V$_{DDB}$	$\overline{SBA}$
< V$_{UVLOA}$	< V$_{UVLOB}$	High
< V$_{UVLOA}$	≥ V$_{UVLOB}$	High
≥ V$_{UVLOA}$	< V$_{UVLOB}$	High
≥ V$_{UVLOA}$	≥ V$_{UVLOB}$	Low

Detailed Description

The MAX14938/MAX14939 isolated PROFIBUS-DP/ RS-485 transceivers provide 2750V$_{RMS}$ (60s) of galvanic isolation between the PROFIBUS-DP/RS-485 cable-side of the transceiver and the UART side. These devices allow fast (20Mbps) communication across an isolation barrier when a large potential exists between grounds on each side of the barrier.

Isolation

Data isolation is achieved using high-voltage capacitors that allow data transmission between the UART side and the Profibus/RS-485 cable side of the transceiver.

Integrated LDO

The MAX14938/MAX14939 include an internal low-dropout regulator with a set 5V (typ) output that is used to power the cable-side of the IC. The output of the LDO is V$_{DDB}$. In addition to powering the transceiver, V$_{DDB}$ can source up to 10mA, allowing external termination resistors to be powered without the need for an external regulator. The LDO has a 300mA (typ) current limit. If the LDO is unused, connect V$_{LDO}$ to GNDB and apply +5V directly to V$_{DDB}$.

True Fail-Safe

The MAX14938/MAX14939 guarantee a logic-high on the receiver output when the receiver inputs are shorted or open, or when connected to a terminated transmission line with all drivers disabled. The receiver threshold is fixed between -50mV and -200mV. If the differential receiver input voltage (V$_A$ – V$_B$) is greater than or equal to -50mV, RXD is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination resistors. Due to the receiver thresholds of the MAX14938/ MAX14939, this results in a logic-high at RXD.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a foldback mode current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Thermal Shutdown

The MAX14938/MAX14939 are protected from overtemperature damage by integrated thermal shutdown circuitry. When the junction temperature (T$_J$) exceeds +160°C (typ), the driver outputs go high-impedance. The device resumes normal operation when T$_J$ falls below +145°C (typ).

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load. A standard driver can drive up to 32 unit-loads. The MAX14938/MAX14939 transceivers have a ¼-unit load receiver, which allows up to 128 transceivers, connected in parallel, on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

Typical Application

The MAX14938/MAX14939 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 10 and Figure 11 show typical network application circuits. To minimize reflections, the bus should be terminated at both ends in its characteristics impedance, and stub lengths off the main line should be kept as short as possible.
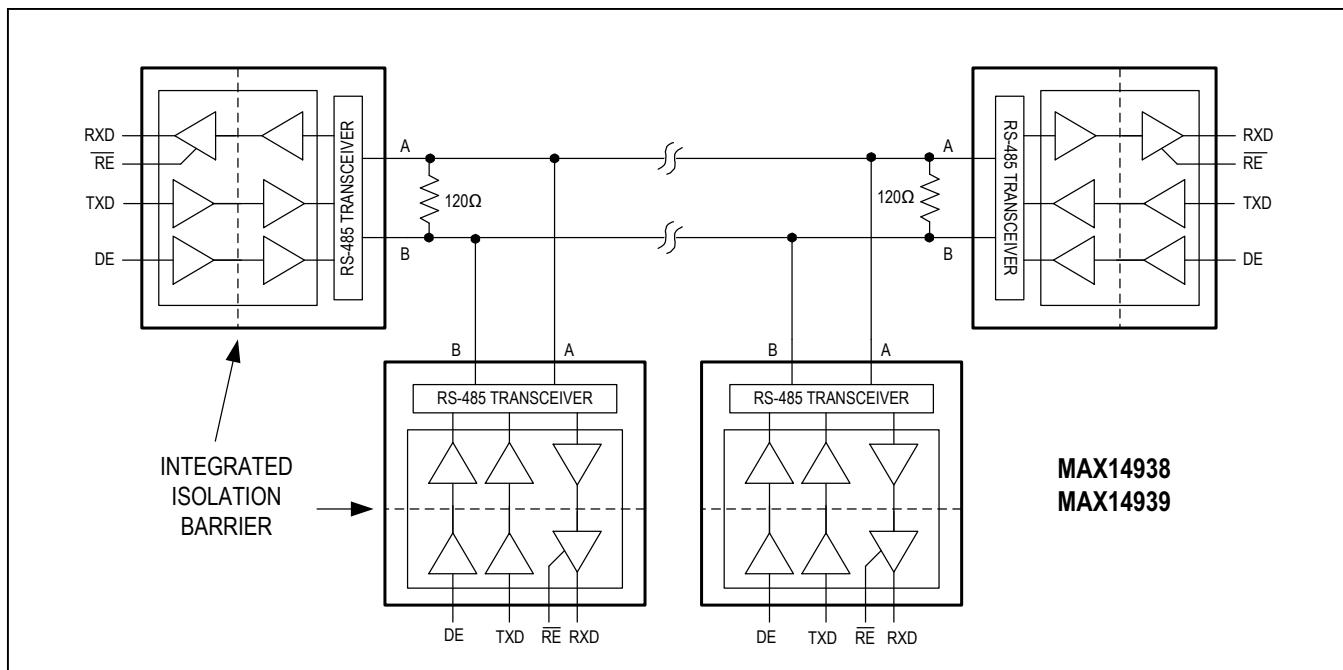
*Figure 10. Typical Isolated Half-Duplex RS-485 Application*
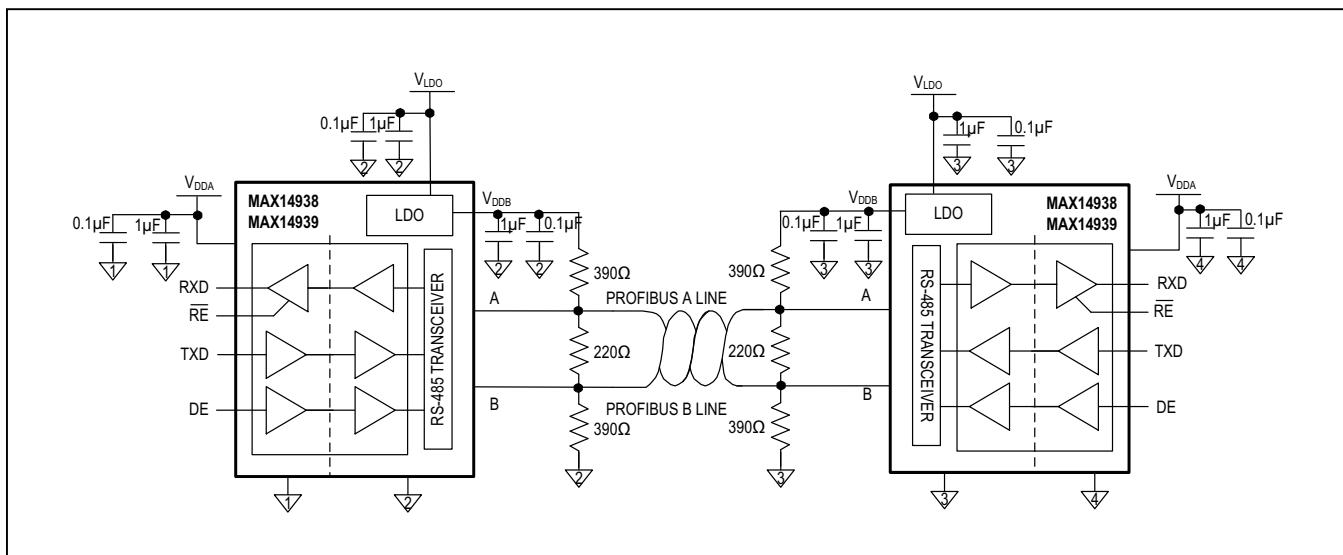
Figure 11. Typical Isolated Profibus Application

Profibus Termination

These devices are designed for driving PROFIBUS-DP terminated networks. The driver maintains 2.1V (min) when driving a worst-case loading condition of two standard 220Ω termination resistors with 390Ω pullups/pulldowns.

Layout Considerations

It is recommended to design an isolation, or "keep-out," channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable-side and UART-side will defeat the isolation.

Ensure that the decoupling capacitors between V$_{DDA}$ and GNDA and between V$_{LDO}$, V$_{DDB}$, and GNDB are located as close as possible to the IC to minimize inductance.

Route important signal lines close to the ground plane to minimize possible external influences. On the cable-side of the MAX14938/MAX14939, it is good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14938/MAX14939 have extra protection against static electricity to both the UART-side and cable-side ground references. The ESD structures withstand high-ESD events during normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

Bypass V$_{DDA}$ to GNDA and bypass V$_{DDB}$ and V$_{LDO}$ to GNDB with 0.1µF and 1µF capacitors to ensure maximum ESD protection.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX14938/MAX14939 are characterized for protection to the cable-side ground (GNDB) to the following limits:

● ±35kV HBM

● ±12kV using the Air-Gap Discharge method specified in IEC 61000-4-2

● ±10kV using the Contact Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model (HBM)

Figure 12 shows the HBM test model, while Figure 13 shows the current waveform it generates when discharged in a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14938/MAX14939 help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

Figure 14 shows the IEC 61000-4-2 model and Figure 15 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.
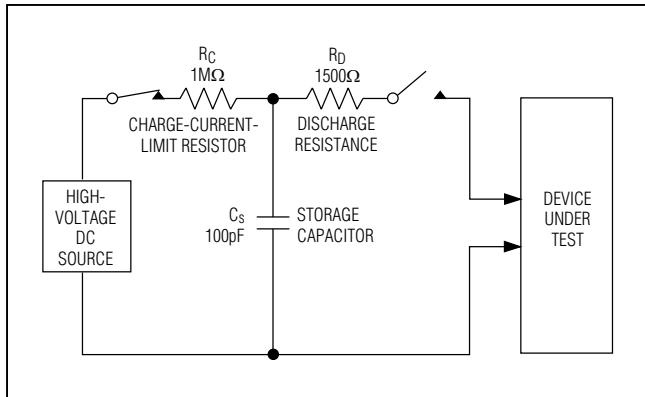
Figure 12. Human Body ESD Test Model
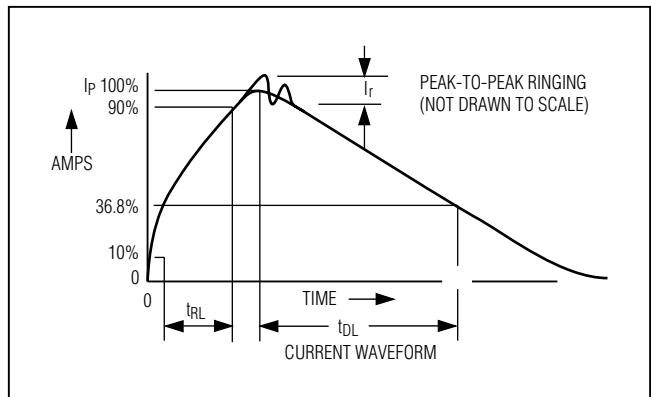

Figure 13. Human Body Current Waveform
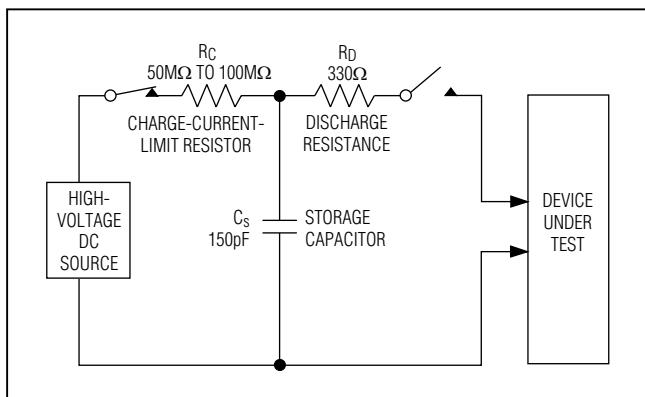
Figure 14. IEC 61000-4-2 ESD Test Model
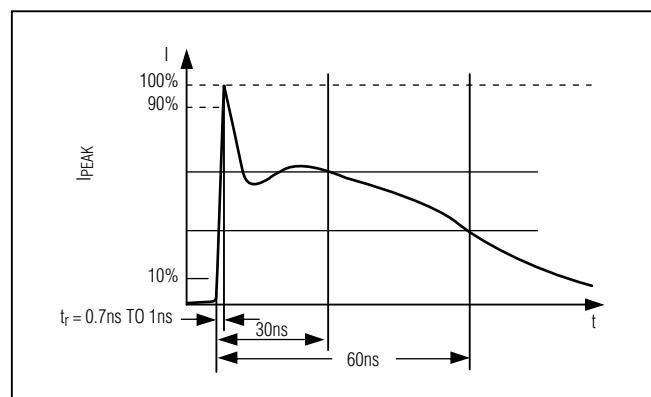
Figure 15. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuit
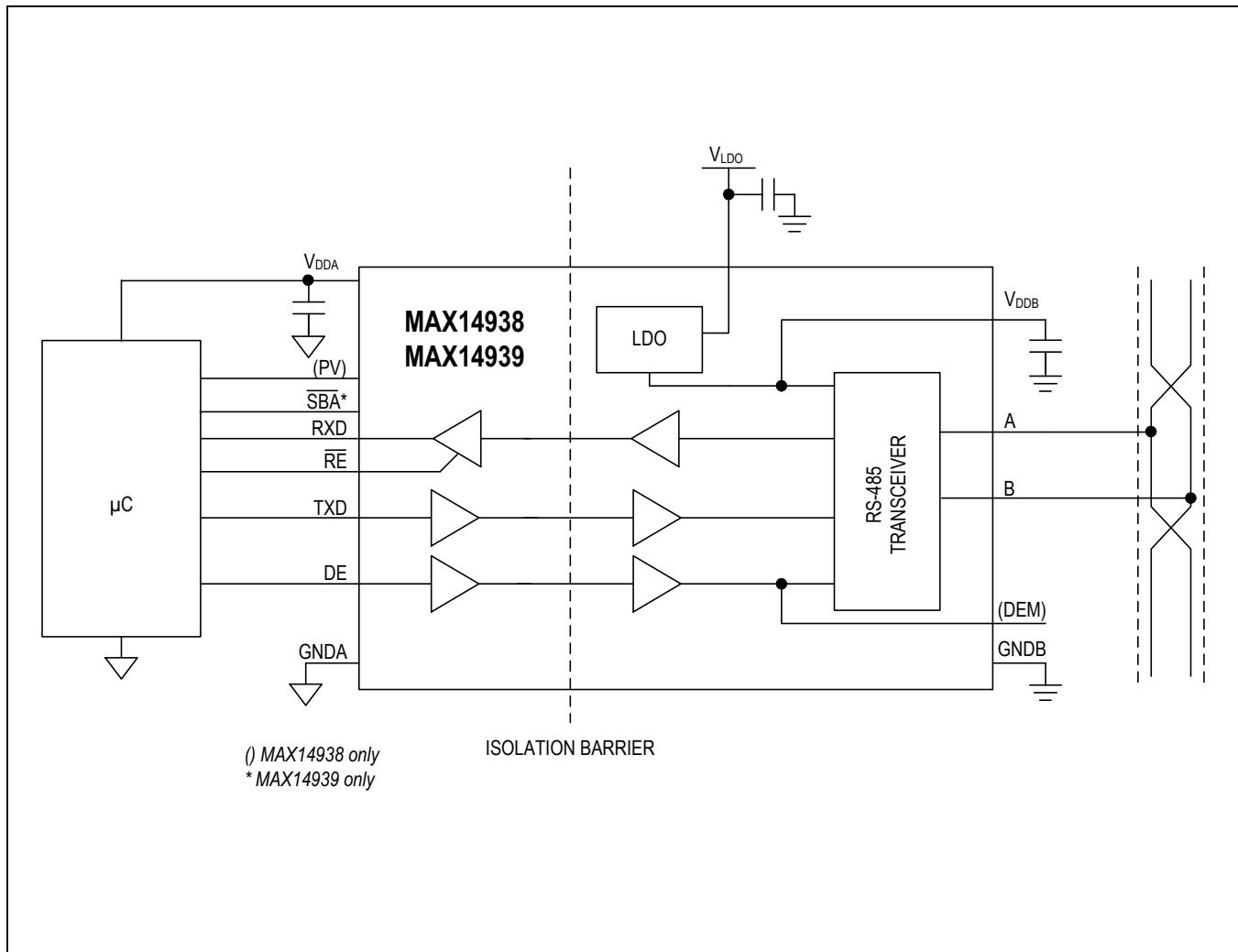
() MAX14938 only
* MAX14939 only

ISOLATION BARRIER

Ordering Information/Selector Guide

PART	DEM	PV	$\overline{SBA}$	TEMP RANGE	PIN-PACKAGE
MAX14938GWE+	√	√	—	-40°C to +105°C	16 SOIC (W)
MAX14938GWE+T	√	√	—	-40°C to +105°C	16 SOIC (W)
MAX14939GWE+	—	—	√	-40°C to +105°C	16 SOIC (W)
MAX14939GWE+T	—	—	√	-40°C to +105°C	16 SOIC (W)

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape & Reel

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SOIC	W16M+9	21-0042	90-0107

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/15	Initial release	—
1	1/17	Updated pending safety approvals	1, 7

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