



NX7002BKXB

60 V, dual N-channel Trench MOSFET

30 June 2015

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Leadless ultra small and ultra thin SMD plastic package 1.1 x 1.0 x 0.37 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

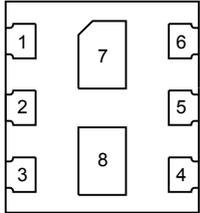
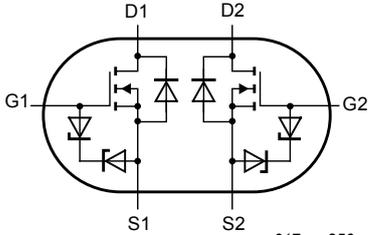
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{sp} = 25\text{ °C}$	-	-	330	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	260	mA
Static characteristics (per transistor)						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 200\text{ mA}; T_j = 25\text{ °C}$	-	2.2	2.8	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN1010B-6 (SOT1216)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

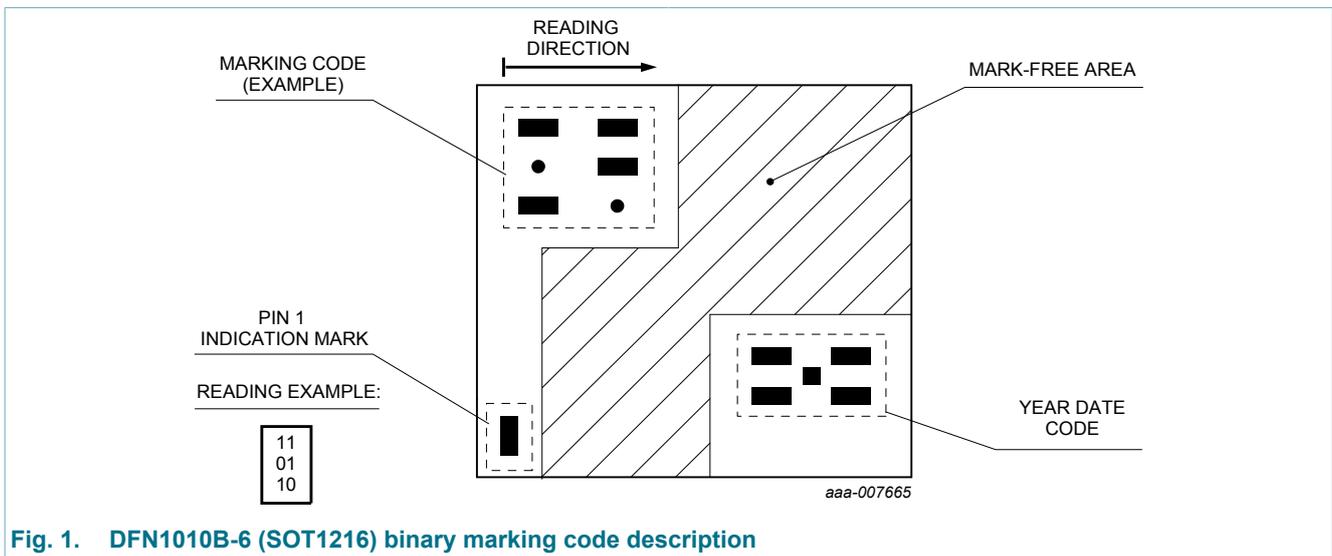
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX7002BKXB	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
NX7002BKXB	00 01 01



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{DS}	drain-source voltage	T _j = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C		-	330	mA
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	260	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	170	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	0.8	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	285	mW
			[1]	-	407	mW
		T _{sp} = 25 °C		-	4032	mW
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	0.2	A
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

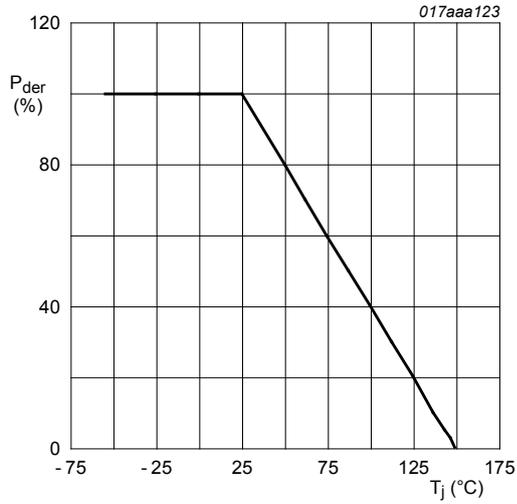


Fig. 2. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

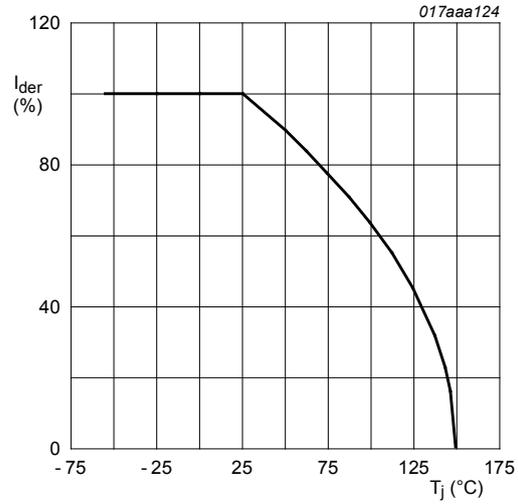
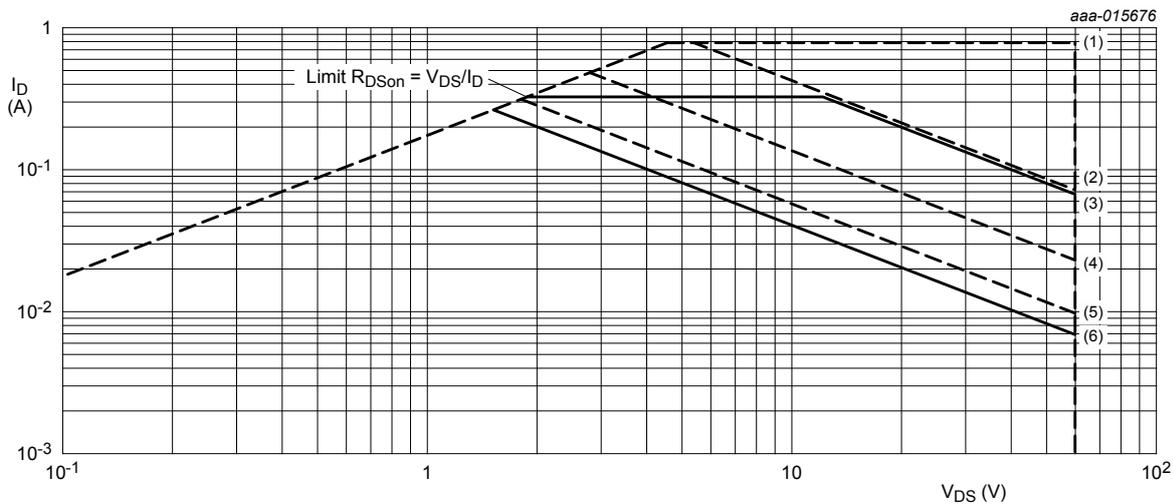


Fig. 3. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$



I_{DM} = single pulse

(1) $t_p = 10 \mu s$

(2) $t_p = 1 ms$

(3) DC; $T_{sp} = 25^{\circ}C$

(4) $t_p = 10 ms$

(5) $t_p = 100 ms$

(6) DC; $T_{amb} = 25^{\circ}C$; drain mounting pad $1 cm^2$

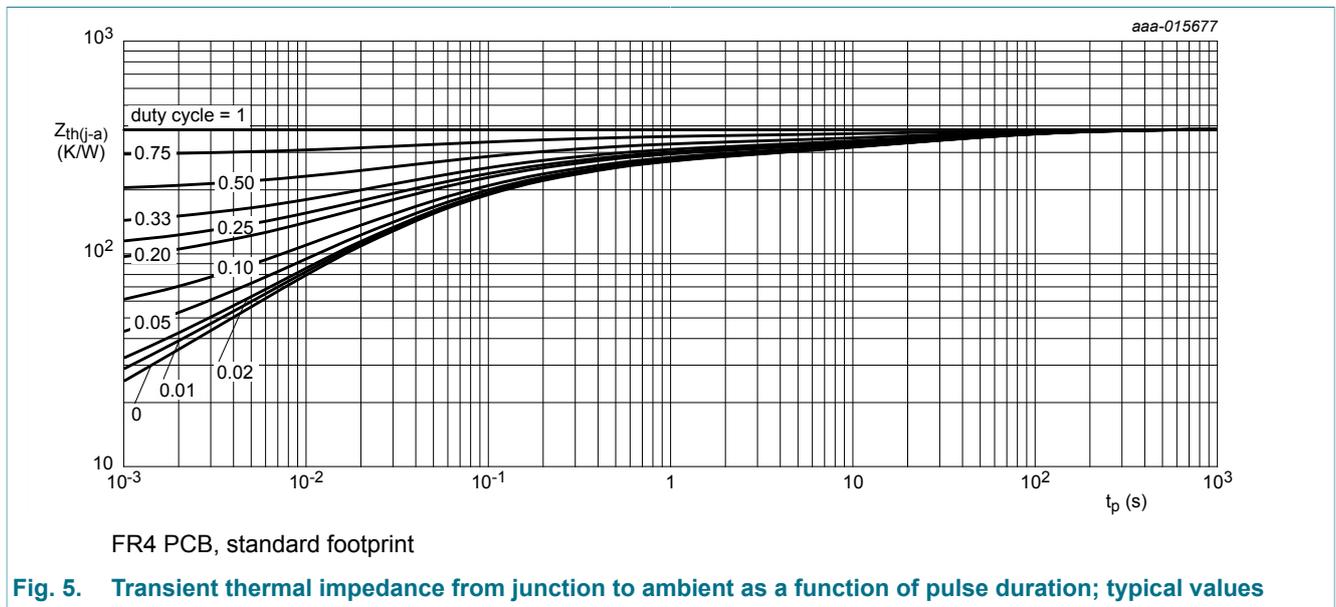
Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

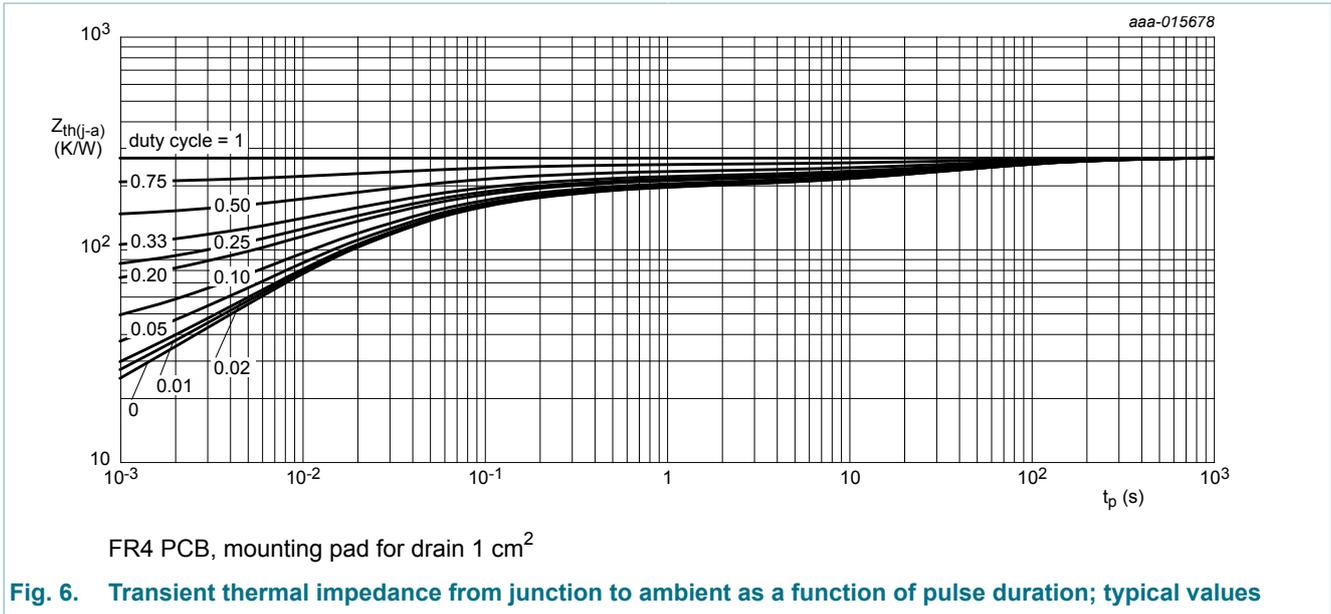
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	276	307	K/W
			[2]	-	381	438	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	27	31	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.1	1.6	2.1	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	0.3	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.2	2.8	Ω
		$V_{GS} = 10 V; I_D = 200 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	4.5	5.7	Ω
		$V_{GS} = 5 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.5	3.2	Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	600	-	mS
R_G	gate resistance	$f = 1 \text{ MHz}$	-	2.5	-	Ω
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 200 \text{ mA}; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$	-	1	-	nC
Q_{GS}	gate-source charge		-	0.12	-	nC
Q_{GD}	gate-drain charge		-	0.18	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	23.6	-	pF
C_{oss}	output capacitance		-	4.6	-	pF
C_{rss}	reverse transfer capacitance		-	3	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 V; I_D = 200 \text{ mA}; V_{GS} = 10 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	4.7	-	ns
t_r	rise time		-	4.3	-	ns
$t_{d(off)}$	turn-off delay time		-	6.9	-	ns
t_f	fall time		-	2.9	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	$I_S = 200 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.87	1.2	V

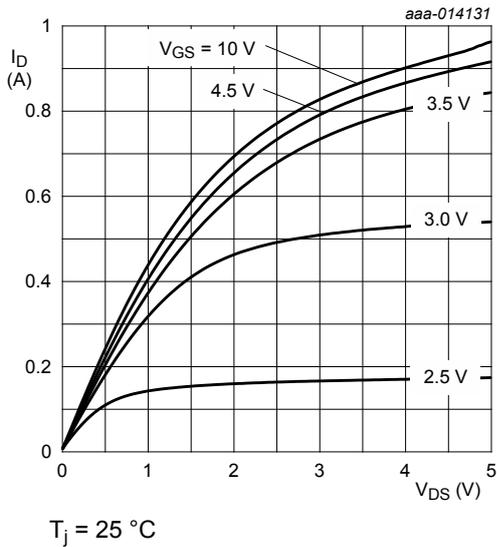


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

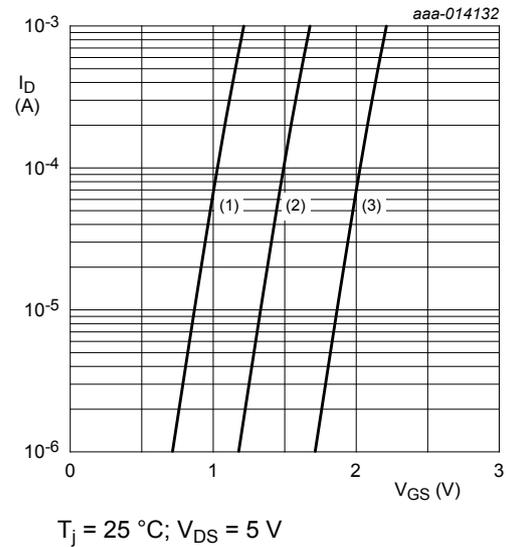


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

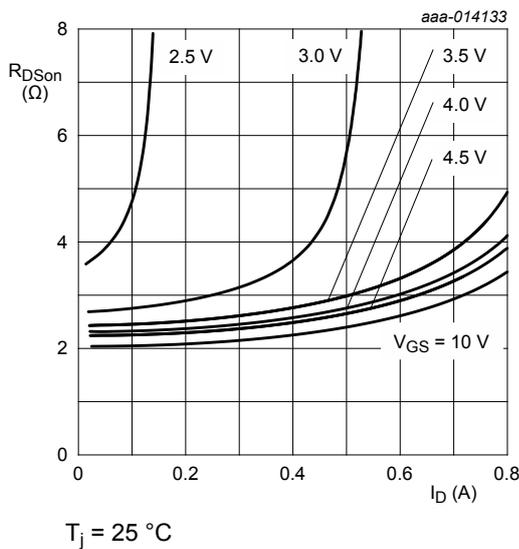


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

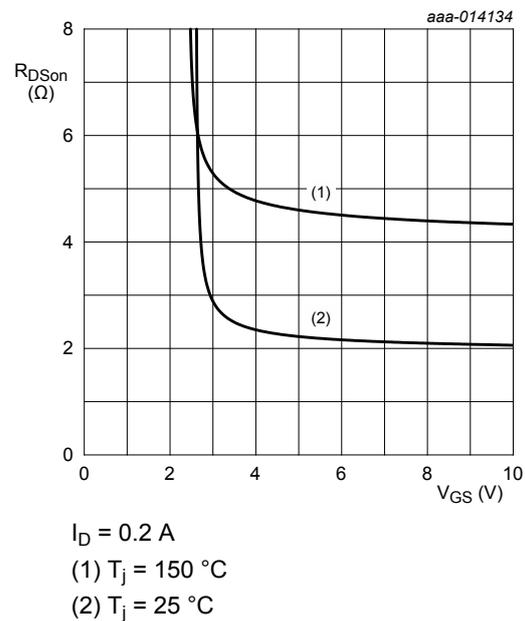
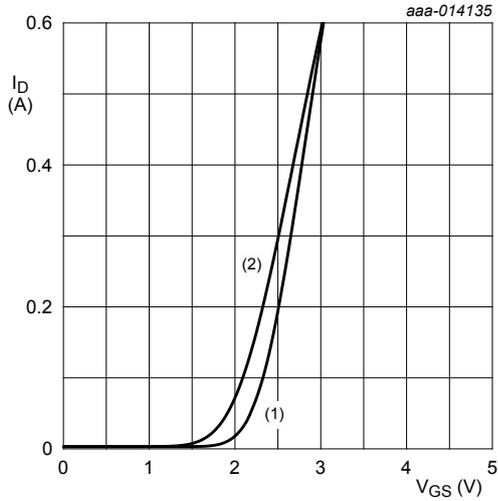


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ }^\circ\text{C}$
 (2) $T_j = 150\text{ }^\circ\text{C}$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

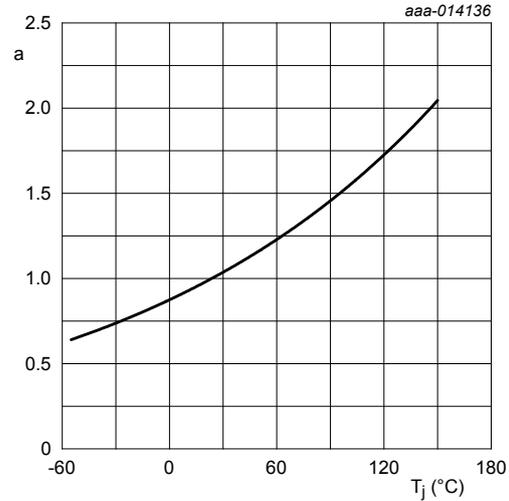
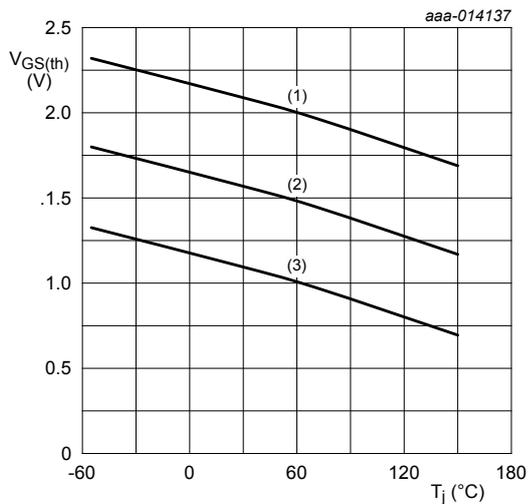


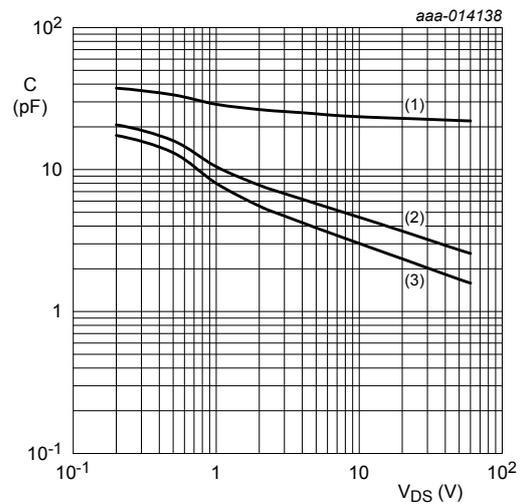
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$



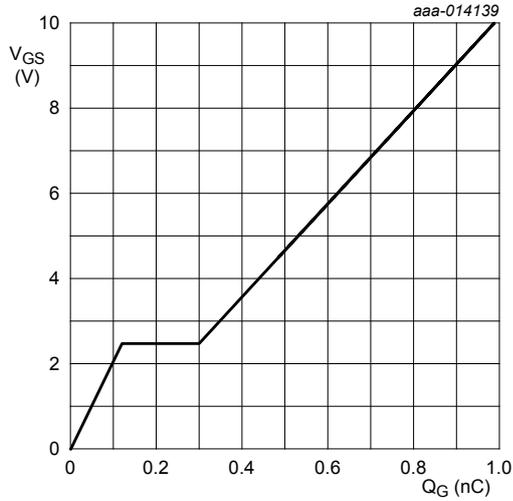
$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.2 \text{ A}$; $V_{DS} = 30 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

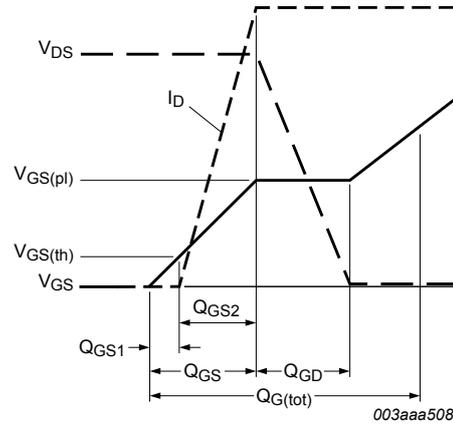
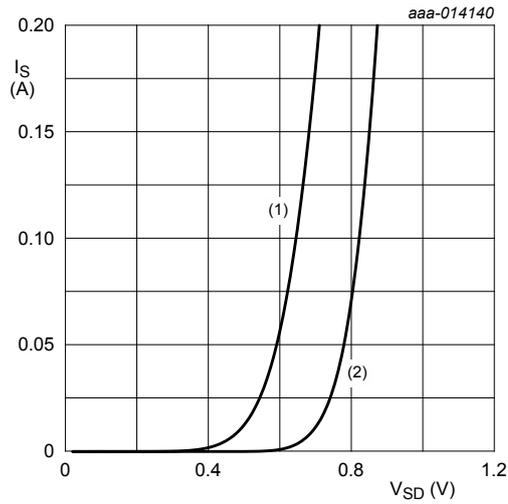


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$
 (1) $T_j = 150 \text{ }^\circ\text{C}$
 (2) $T_j = 25 \text{ }^\circ\text{C}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

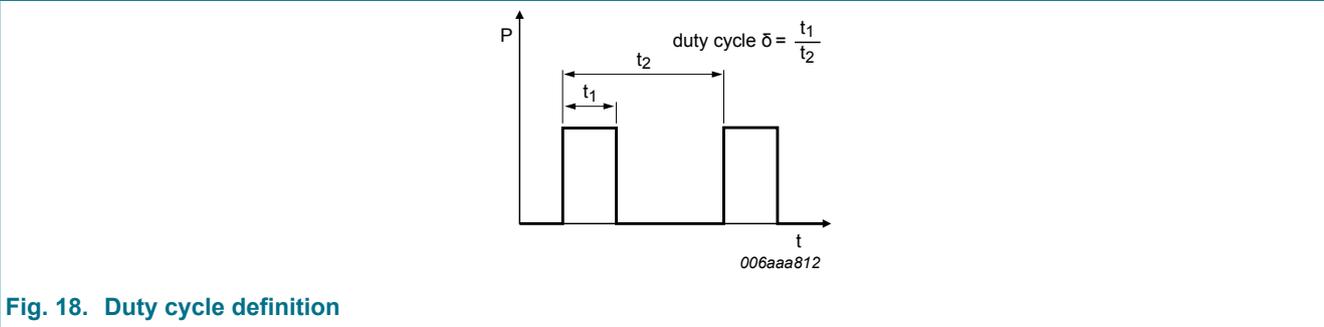
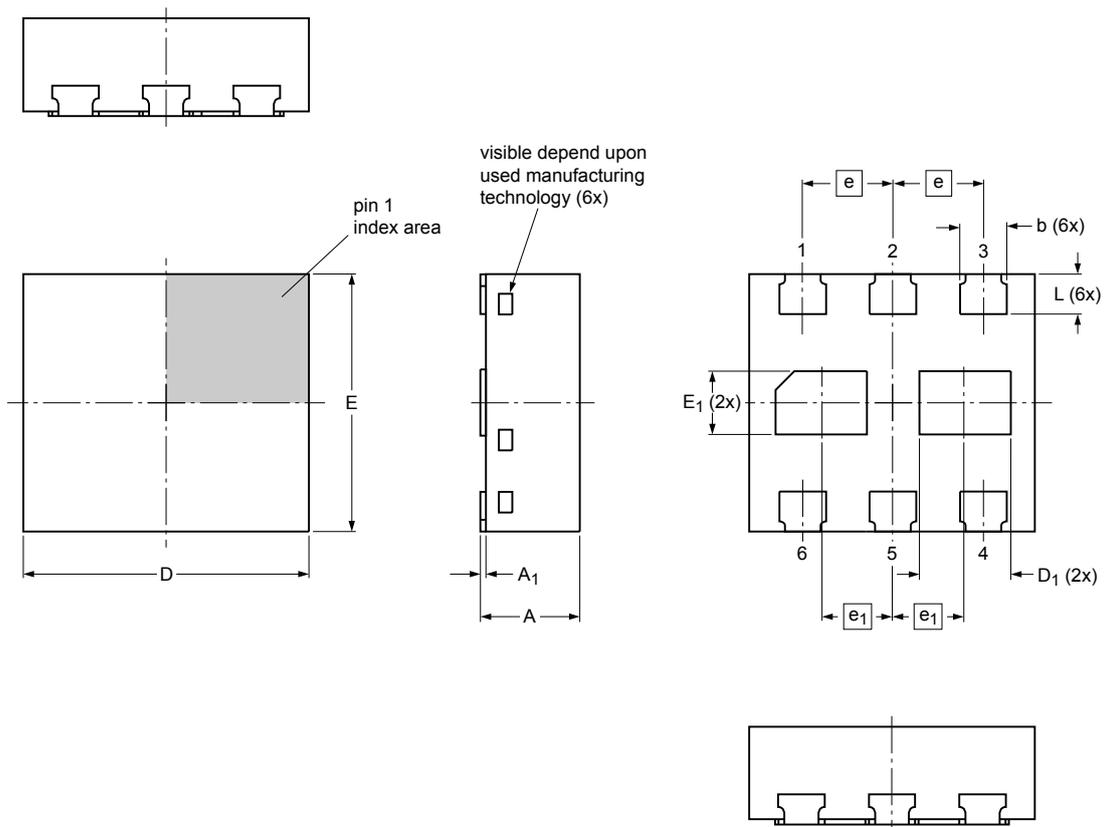


Fig. 18. Duty cycle definition

12. Package outline

DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1216



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	D	D ₁	E	E ₁	e	e ₁	L
min	0.34		0.15	1.05	0.32	0.95	0.22			0.125
mm nom	0.37		0.18	1.10	0.35	1.00	0.25	0.35	0.275	0.155
max	0.40	0.04	0.23	1.15	0.40	1.05	0.30			0.205

Note

1. Dimension A is including plating thickness.

sot1216_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1216					-13-03-05- 13-03-06

Fig. 19. Package outline DFN1010B-6 (SOT1216)

13. Soldering

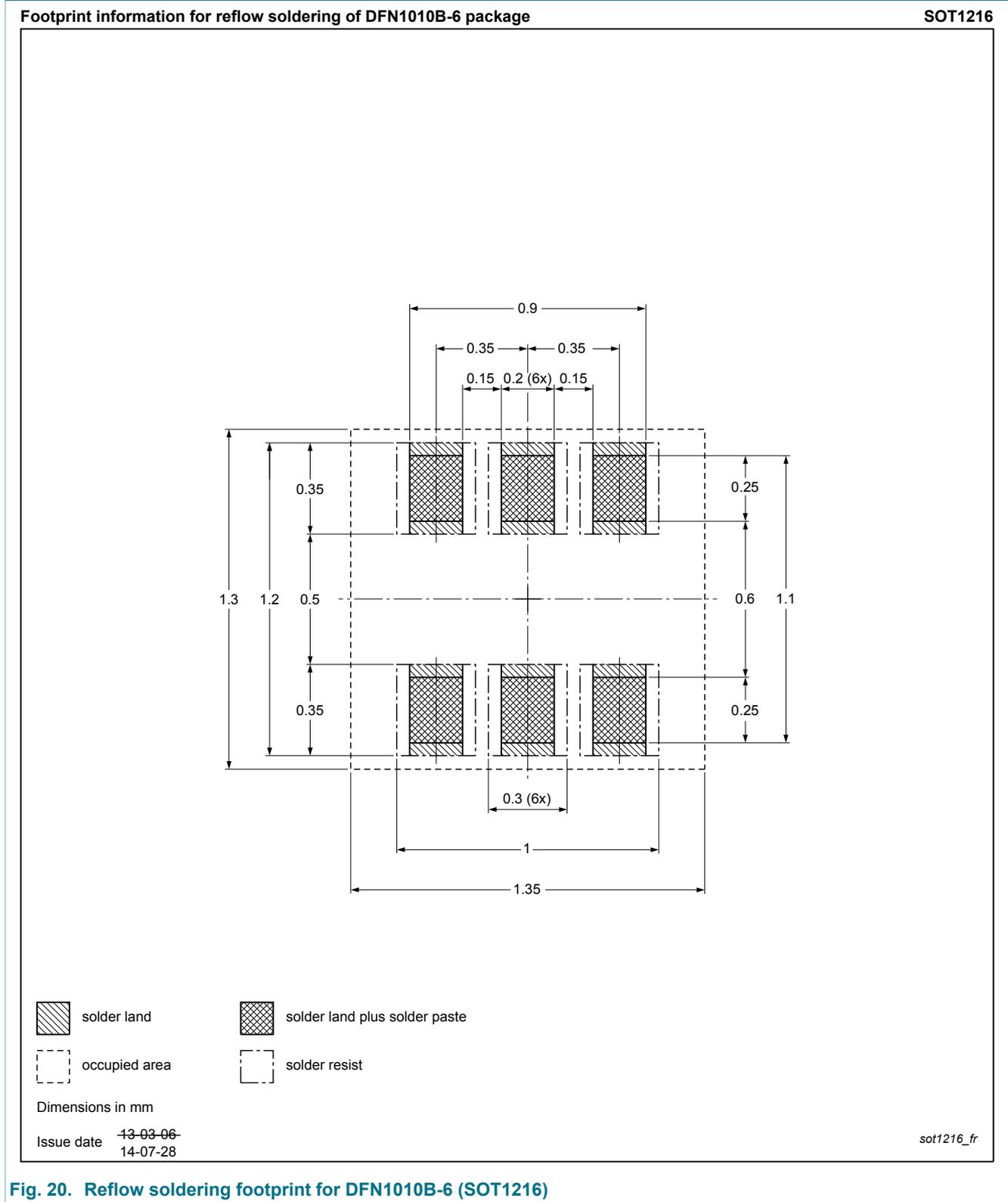


Fig. 20. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX7002BKXB v.2	20150630	Product data sheet	-	NX7002BKXB v.1
Modification:	<ul style="list-style-type: none">Change of binary marking code position			
NX7002BKXB v.1	20141210	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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